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**UTILITY
PATENT APPLICATION
TRANSMITTAL**

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Atty. Docket No.	X-735 US
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First Inventor or Appl. Identifier	John D. Logue
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Title	Synchronized Multi-Output Digital Clock Manager
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Express Mail Label No.	EL539650632US
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APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO:

Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. ☒ *Fee Transmittal Form (e.g., PTO/SB/17)
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- | | | | |
|--|----------------------|---------------|-----------|
| 2. X | Specification | [Total Pages] | 53 |
| <i>(preferred arrangement set forth below)</i> | | | |
| <ul style="list-style-type: none">- Descriptive title of the invention- Cross References to Related Applications- Statement Regarding Fed sponsored R & D- Reference to sequent listing, a table, or a computer program listing appendix- Background of the invention- Brief Summary of the invention- Brief Description of the Drawings <i>(if filed)</i>- Detailed Description- Claim(s) | | | |

6. ☐ CD-ROM or CD-R in duplicate, large table or Computer Program (*Appendix*)
7. ☐ Nucleotide and/or Amino Acid Sequence Submission (*if applicable, all necessary*)
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3. ☒ Drawing(s) (35 USC 113) [Total Sheets

4. Oath or Declaration [Total Pages 2]

- a. ☒ Newly ~~submitted~~ (original or copy)
- b. ☐ Copy from a prior application (37 CFR § 1.63(d))
(for continuation/divisional with Box 16 completed)
- i. ☐ DELETION OF INVENTOR(S)
Signed statement attached deleting
inventor(s) named in the prior application,
see 37 CFR § 1.63(d)(2) and 1.33(b).

5. ☐ Application Data Sheet. See 37 CFR 1.76

ACCOMPANYING APPLICATION PARTS

8. ☐ Assignment Papers (cover sheet & document(s))
9. ☐ 37 CFR §3.73(b) Statement ☐ Power of Attorney
(when there is an assignee)
10. ☐ English Translation Document (if applicable)
11. ☐ Information Disclosure ☐ Copies of IDS
Statement (IDS)/PTO-1449 Citations
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**FEE TRANSMITTAL
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106	320	Design filing fee	
107	490	Plant filing fee	
108	710	Reissue filing fee	
114	150	Provisional filing fee	

SUBTOTAL (1) (\$ 710.00)**2. EXTRA CLAIM FEES**

	Extra	Fee from below	Fee Paid
Total Claims 22 - 20** =	2	18	\$36
Indep Claims 02 - 3** =	-1		\$0
Multiple Dependent			

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Fee Code	Fee (\$)	Fee Description
103	18	Claims in excess of 20
102	80	Independent claims in excess of 3
104	270	Multiple dependent claim, if not paid
109	80	**Reissue independent claims over original patent
110	18	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) (\$ 36.00)**FEE CALCULATION (continued)****3. ADDITIONAL FEES****Large Entity**

Code	Fee (\$)	Fee Description	Fee Paid
105	130	Surcharge - late filing fee or oath	
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147	2,520	For filing a request for reexamination	
112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	Requesting publication of SIR after Examiner action	
115	110	Extension for reply within first month	
116	390	Extension for reply within second month	
117	890	Extension for reply within third month	
118	1,390	Extension for reply within fourth month	
128	1,890	Extension for reply within fifth month	
119	310	Notice of Appeal	
120	310	Filing a brief in support of an appeal	
121	270	Request for oral hearing	
138	1,510	Petition to institute a public use proceeding	
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1 SYNCHRONIZED MULTI-OUTPUT DIGITAL CLOCK MANAGER

2
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6
7 FIELD OF THE INVENTION8
9 The present invention relates to digital clocking
10 circuits for digital electronics. More specifically, the
11 present invention relates to digital clock managers capable
12 of generating multiple phase-locked output clock signals of
13 different frequencies.
1415 BACKGROUND OF THE INVENTION16
17 Synchronous digital systems, including board level
18 systems and chip level systems, rely on one or more clock
19 signals to synchronize elements across the system.
20 Typically, one or more clock signals are distributed across
21 the system on one or more clock lines. However, due to
22 various problems such as clock buffer delays, high
23 capacitance of heavily loaded clock lines, and propagation
24 delays, the edges of a clock signal in different parts of
25 the system may not be synchronized. The time difference
26 between a rising (or falling) edge in one part of the system
27 with the corresponding rising (or falling) edge in another
28 part of the system is referred to as "clock skew".29 Clock skew can cause digital systems to malfunction.
30 For example, it is common for circuits in digital systems to
31 have a first flip-flop output driving a second flip-flop
32 input. With a synchronized clock signal on the clock input
33 terminal of both flip-flops, the data in the first flip-flop
34 is successfully clocked into the second flip-flop. However,
35 if the active edge on the second flip flop is delayed by
36 clock skew, the second flip-flop might not capture the data

1 from the first flip-flop before the first flip-flop changes
2 state.

3 Delay lock loops are used in digital systems to
4 minimize clock skew. Delay lock loops typically use delay
5 elements to synchronize the active edges of a reference
6 clock signal in one part of the system with a feedback clock
7 signal from a second part of the system. Figure 1 shows a
8 block diagram of a conventional delay lock loop 100 coupled
9 to logic circuits 190. Delay lock loop 100, which comprises
10 a delay line 110 and a phase detector 120, receives a
11 reference clock signal REF_CLK and drives an output clock
12 signal O_CLK.

13 Delay line 110 delays reference clock signal REF_CLK by
14 a variable propagation delay D before supplying output clock
15 signal O_CLK. Thus, each clock edge of output clock signal
16 O_CLK lags a corresponding clock edge of reference clock
17 signal REF_CLK by propagation delay D (see Figure 2(a)).
18 Phase detector 120 controls delay line 110, as described
19 below. Delay line 110 is capable of producing a minimum
20 propagation delay D_MIN and a maximum propagation delay
21 D_MAX.

22 Before output clock signal O_CLK reaches logic circuits
23 190, output clock signal O_CLK is skewed by clock skew 180.
24 Clock skew 180 can be caused by delays in various clock
25 buffers (not shown) or propagation delays on the clock
26 signal line carrying output clock signal O_CLK (e.g., due to
27 heavy loading on the clock signal line). To distinguish
28 output clock signal O_CLK from the skewed version of output
29 clock signal O_CLK, the skewed version is referred to as
30 skewed clock signal S_CLK. Skewed clock signal S_CLK drives
31 the clock input terminals (not shown) of the clocked
32 circuits within logic circuits 190. Skewed clock signal
33 S_CLK is also routed back to delay lock loop 100 on a
34 feedback path 170. Typically, feedback path 170 is
35 dedicated specifically to routing skewed clock signal S_CLK
36 to delay lock loop 110. Therefore, any propagation delay on

1 feedback path 170 is minimal and causes only negligible
2 skewing.

3 Figure 2(a) provides a timing diagram of reference
4 clock signal REF_CLK, output clock signal O_CLK, and skewed
5 clock signal S_CLK. All three clock signals have the same
6 frequency F_{REF} (not shown) and period P_{REF} , and all are
7 active-high (i.e., the rising edge is the active edge).
8 Since output clock signal O_CLK is delayed by propagation
9 delay D , a clock edge 220 of output clock signal O_CLK lags
10 corresponding clock edge 210 of reference clock signal
11 REF_CLK by propagation delay D . Similarly, a clock edge 230
12 of skewed clock signal S_CLK lags corresponding clock edge
13 220 of output clock signal O_CLK by a propagation delay
14 SKEW, which is the propagation delay caused by clock skew
15 180 (Figure 1). Therefore, clock edge 230 of skewed clock
16 signal S_CLK lags clock edge 210 of reference clock signal
17 REF_CLK by a propagation delay $DSKEW$, which is equal to
18 propagation delay D plus propagation delay SKEW.

19 Delay lock loop 100 controls propagation delay D by
20 controlling delay line 110. However, delay line 110 cannot
21 create negative delay; therefore, clock edge 230 cannot be
22 synchronized to clock edge 210. Fortunately, clock signals
23 are periodic signals. Therefore, delay lock loop 100 can
24 synchronize reference clock signal REF_CLK and skewed clock
25 signal S_CLK by further delaying output clock signal O_CLK
26 such that clock edge 240 of skewed clock signal S_CLK is
27 synchronized with clock edge 210 of reference clock signal
28 REF_CLK. As shown in Figure 2(b), propagation delay D is
29 adjusted so that propagation delay $DSKEW$ is equal to period
30 P . Specifically, delay line 110 is tuned so that
31 propagation delay D is increased until propagation delay D
32 equals period P minus propagation delay SKEW. Although
33 propagation delay $DSKEW$ could be increased to any multiple
34 of period P to achieve synchronization, most delay lock
35 loops do not include a delay line capable of creating such a
36 large propagation delay.

Phase detector 120 (Figure 1) controls delay line 110 to regulate propagation delay D. The actual control mechanism for delay lock loop 100 can differ. For example, in one version of delay lock loop 100, delay line 110 starts with a propagation delay D equal to minimum propagation delay D_MIN, after power-on or reset. Phase detector 110 then increases propagation delay D until reference clock signal REF_CLK is synchronized with skewed clock signal S_CLK. In another system, delay lock loop 100 starts with a propagation delay D equal to the average of minimum propagation delay D_MIN and maximum propagation delay D_MAX, after power-on or reset. Phase detector 120 then determines whether to increase or decrease (or neither) propagation delay D to synchronize reference clock signal REF_CLK with skewed clock signal S_CLK. For example, phase detector 120 would increase propagation delay D for the clock signals depicted in Figure 2(a). However, phase detector 120 would decrease propagation delay D for the clock signals depicted in Figure 2(c).

In Figure 2(c), skewed clock signal S_CLK is said to "lag" reference clock signal REF_CLK, because the time between a rising edge of reference clock signal REF_CLK and the next rising edge of skewed clock signal S_CLK is less than the time between a rising edge of skewed clock signal S_CLK and the next rising edge of reference clock signal REF_CLK. However, in Figure 2(a), reference clock signal REF_CLK is said to "lag" skewed clock signal S_CLK, because the time between a rising edge of skewed clock signal S_CLK and the next rising edge of reference clock signal REF_CLK is less than the time between a rising clock edge of reference clock signal REF_CLK and the next rising clock edge of skewed clock signal S_CLK. Alternatively, in Figure 2(a) skewed clock signal S_CLK could be said to "lead" reference clock signal REF_CLK.

After synchronizing reference clock signal REF_CLK and skewed clock signal S_CLK, delay lock loop 100 monitors

1 reference clock signal REF_CLK and skewed clock signal S_CLK
2 and adjusts propagation delay D to maintain synchronization.
3 For example, if propagation delay SKEW increases, perhaps
4 caused by an increase in temperature, delay lock loop 100
5 must decrease propagation delay D to compensate.
6 Conversely, if propagation delay SKEW decreases, perhaps
7 caused by a decrease in temperature, delay lock loop 100
8 must increase propagation delay D to compensate. The time
9 in which delay lock loop 100 is attempting to first
10 synchronize reference clock signal REF_CLK and skewed clock
11 signal S_CLK, is referred to as lock acquisition. The time
12 in which delay lock loop 100 is attempting to maintain
13 synchronization is referred to as lock maintenance. The
14 value of propagation delay D at the end of lock acquisition,
15 i.e. when synchronization is initially established, is
16 referred to as initial propagation delay ID.

17 Further complications with clock skew exists in complex
18 digital systems, such as microprocessors and FPGAs, that
19 have multiple clock signals at different frequencies. For
20 example, in some microprocessors, internal circuits are
21 clocked by a first clock signal at a first clock frequency
22 while input/output (I/O) circuits are clocked by a second
23 clock signal at a second clock frequency. Typically, the
24 second clock frequency is slower than the first clock
25 frequency.

26 Most systems use one clock generating circuit to
27 generate a first clock signal and a specialized circuit to
28 derive other clock signals from the first clock signal. For
29 example, clock dividers are used to generate one or more
30 clock signals of lower clock frequencies from a reference
31 clock signal. Typically, clock dividers divide the
32 frequency of the reference clock signal by an integer value.
33 Conversely, clock multipliers are used to generate one or
34 more clock signals of higher clock frequencies from the
35 reference clock signal. Combining clock multipliers with
36 clock dividers provide clocking circuits which can generate

one or more clock signals having frequencies that are fractional values of the frequency of the reference clock signal.

Thus, a clocking circuit is typically coupled to reference clock signal REF_CLK to generate a frequency adjusted clock signal FREQ_CLK. However, the clocking circuits add additional skew due to propagation delay and gate switching times. Consequently, frequency adjusted clock signal FREQ_CLK may be skewed compared to both reference clock signal REF_CLK and output clock signal O_CLK. Hence, there is a need for a method and circuits that can compensate for skew in both an output clock signal and a frequency adjusted clock signal.

SUMMARY

The present invention provides a digital clock manager that generates a deskewed output clock signal as well as a deskewed frequency adjusted clock signal. Specifically, the output clock signal causes a skewed clock signal to be synchronized with a reference clock signal. The frequency adjusted clock signal is synchronized with the output clock signal during concurrences. Generally the frequency adjusted clock signal is driven to a selected clock frequency which is equal to the clock frequency of the output clock signal multiplied by a multiplier M and divided by a divider D, where M and D are natural numbers. When the frequency of the frequency adjusted clock signal is equal to the selected frequency and the frequency adjusted clock signal is in phase with the output clock signal, every Mth rising edge of the frequency adjusted clock signal aligns with a rising edge of the output clock signal. The alignments are commonly referred to as concurrences.

One embodiment of the digital clock manager includes a delay lock loop (DLL) and a digital frequency synthesizer (DFS). The delay lock loop is configured to generate an output clock signal that synchronizes a skewed clock signal

1 with a reference clock signal. The delay lock loop also
2 generates a synchronizing clock signal, which is provided to
3 the digital frequency synthesizer. The delay lock loop has
4 a DLL output circuit that generates the output clock signal,
5 which lags the synchronizing clock signal by a DLL output
6 delay. In the digital frequency synthesizer, a DFS output
7 circuit generates a frequency adjusted clock signal in which
8 an active edge of the frequency adjusted clock signal lags
9 an active edge of the synchronizing clock signal by a DFS
10 output delay during a concurrence period. By matching the
11 DLL output delay with the DFS output delay, the output clock
12 signal and the frequency adjusted clock signals are
13 synchronized.

14 The present invention will be more fully understood in
15 view of the following description and drawings.

16 17 BRIEF DESCRIPTION OF THE DRAWINGS

18 Figure 1 is a block diagram of a system using a
19 conventional delay lock loop.

20 Figures 2(a), 2(b) and 2(c) are timing diagrams for the
21 system of Figure 1.

22 Figure 3 is a block diagram of a digital clock manager
23 in accordance with one embodiment of the present invention.

24 Figure 4 is a block diagram of a digital clock manager
25 in accordance with one embodiment of the present invention.

26 Figure 5 is a block diagram of a digital clock manager
27 in accordance with one embodiment of the present invention.

28 Figure 6 is a block diagram of a system using an
29 embodiment of a delay lock loop in accordance with the
30 present invention.

31 Figure 7 is a timing diagram for the delay lock loop of
32 Figure 6.

33 Figure 8 illustrates a lock window as used in
34 accordance with one embodiment of the present invention.

1 Figure 9 is a block diagram of an embodiment of a
2 clock phase shifter in accordance with the present
3 invention.

4 Figure 10 is a block diagram of another embodiment of a
5 clock phase shifter in accordance with the present
6 invention.

7 Figure 11 is a block diagram of an output generator in
8 accordance with the present invention.

9 Figure 12 is a state diagram for an embodiment of a
10 controller in accordance with the present invention.

11 Figure 13 is a block diagram of a system using another
12 embodiment of a delay lock loop in accordance with the
13 present invention.

14 Fig. 14(a) is a block diagram of a variable clocking
15 circuit in accordance with one embodiment of the present
16 invention.

17 Fig. 14(b) is a timing diagram for the variable
18 clocking circuit of Fig. 14(a).

19 Fig. 15 is schematic diagram of a variable digital
20 oscillator in accordance with one embodiment of the present
21 invention.

22 Fig. 16 is a timing diagram for the variable clocking
23 circuit of Fig. 14(a) using the digital oscillator of Fig.
24 15.

25 Fig. 17 is a block diagram of an oscillator control
26 circuit in accordance with one embodiment of the present
27 invention.

28 Fig. 18 is a block diagram of an initialization circuit
29 in accordance with a second embodiment of the present
30 invention.

31 Fig. 19 is a timing diagram for the variable clocking
32 circuit of Fig. 14(a) using a delay line fine tuning
33 controller.

34 Fig. 20 is a block diagram of a delay line fine tuning
35 controller in accordance with one embodiment of the present
36 invention.

Fig. 21 is a block diagram of a modulo-M delta sigma circuit in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION

Fig. 3 is a block diagram of a digital clock manager 300 in accordance with one embodiment of the present invention. Digital clock manager 300, which receives a reference clocks signal REF_CLK and a skewed clock signal S_CLK, generates an output clock signal O_CLK, which causes skewed clock signal S_CLK to be synchronized with reference clock signal REF_CLK, and a frequency adjusted clock signal FREQ_CLK which is phase locked with output clock signal O_CLK during concurrences. Generally, frequency adjusted clock signal FREQ_CLK has an adjusted frequency F_ADJ which is equal to the frequency of output clock signal O_CLK multiplied by a multiplier M and divided by a divider D. If frequency adjusted clock signal FREQ_CLK is in phase with clock signal O_CLK, every Mth rising edge of frequency adjusted clock signal FREQ_CLK aligns with a rising edge of output clock signal O_CLK. The alignments are commonly referred to as concurrences. Reference clock signal REF_CLK and output clock signal O_CLK have the same frequency. For clarity, reference frequency F_REF is used to denote the frequency of both reference clock signal REF_CLK and output clock signal O_CLK.

The embodiment of Fig. 3 includes a delay lock loop 310 and a digital frequency synthesizer 320. While specific embodiments of delay lock loop 310 and digital frequency synthesizer 320 are described below, the principles of the present invention can be adapted for use with almost any delay lock loop and any digital frequency synthesizer. Thus, the description with respect to digital clock manager 300 describes delay lock loop 310 and digital frequency synthesizer 320 in general terms. One skilled in the art can adapt the principles of the present invention to create

1 a digital clock manager with a variety of delay lock loops
2 and digital frequency synthesizers.

3 Delay Lock Loop 310 includes DLL clocking circuit 312
4 and DLL output circuit 314. DLL clocking circuit 312
5 generates a synchronizing clock signal SYNCH_CLK, which is
6 provided to DLL output circuit 314 and DFS output circuit
7 324 of digital frequency synthesizer 320. Generally,
8 synchronizing clock signal SYNCH_CLK has a frequency equal
9 to frequency F_REF of reference clock signal REF_CLK and
10 output clock signal O_CLK. DLL output circuit 314 drives
11 output clock signal O_CLK. DLL output circuit 314
12 introduces a DLL output delay 316 between synchronizing
13 clock signal SYNCH_CLK and output clock circuit O_CLK.
14 Specifically, output clock signal O_CLK lags synchronizing
15 clock signal SYNCH_CLK by DLL output delay 316. DLL
16 clocking circuit 312 and DLL output circuit 314 together
17 synchronizes skewed clock signal S_CLK with reference clock
18 signal REF_CLK. A specific embodiment of delay lock loop
19 310 used in one embodiment of the present invention is
20 described below.

21 Digital frequency synthesizer 320 receives synchronized
22 clock signal SYNCH_CLK and generates frequency adjusted
23 clock signal FREQ_CLK having adjusted frequency F_ADJ, which
24 is equal to the frequency of output clock signal O_CLK
25 multiplied by a multiplier M and divided by a divider D. As
26 shown in Fig. 3, digital frequency synthesizer 320 includes
27 a DFS clocking circuit 322 and a DFS output circuit 324.
28 DFS output circuit 324 drives frequency adjusted clock
29 signal FREQ_CLK and introduces a DFS output delay 326
30 between frequency adjusted clock signal FREQ_CLK and
31 synchronizing clock signal SYNCH_CLK. Specifically, during
32 concurrence periods of synchronizing clock signal SYNCH_CLK
33 with frequency adjusted clock signal FREQ_CLK, an active
34 edge of frequency adjusted clock signal FREQ_CLK lags an
35 active edge of synchronizing clock signal SYNCH_CLK by DFS
36 output delay 326. DFS clocking circuit 322 and DFS output

1 circuit 324 combine to perform the frequency adjustments
2 necessary to generate frequency adjusted clock signal
3 FREQ_CLK.

4 Because output clock signal O_CLK lags synchronizing
5 clock signal SYNCH_CLK by DLL output delay 316 and frequency
6 adjusted clock signal FREQ_CLK lags synchronizing clock
7 signal SYNCH_CLK by DFS output delay 326, frequency adjusted
8 clock signal FREQ_CLK can be synchronized with output clock
9 signal O_CLK by matching DLL output delay 316 with DFS
10 output delay 326. Thus, in accordance with some embodiments
11 of the invention, the components of DFS output circuit 324
12 and DLL output circuit 314 are chosen to match DLL output
13 delay 316 with DFS output delay 326. For example, in some
14 embodiments of the present invention, DLL output circuit 314
15 and DFS output circuit 324 comprise the identical
16 components. Furthermore, in some embodiments of the present
17 invention, the layout and routing for DLL output circuit 314
18 closely match the layout and routing for DFS output circuit
19 324. By matching components, layout, and routing, these
20 embodiments of the present invention can achieve near-
21 perfect matching between DLL output delay 316 and DFS output
22 delay 326.

23 However, some embodiments of the present invention can
24 not achieve suitable matching of DFS output delay 326 and
25 DLL output delay 316. For these embodiments, additional
26 delay circuitry can be used to synchronize output clock
27 signal O_CLK and frequency adjusted clock signal FREQ_CLK.
28 Fig. 4 is a block diagram of a digital clock manager 400
29 using variable delay circuits 410 and 420 in accordance with
30 one embodiment of the present invention. Because, digital
31 clock manager 400 is similar to digital clock manager 300,
32 similar reference numerals are used for similar elements.
33 In addition, descriptions of the repeated elements are
34 omitted for brevity. Variable delay circuit 410 is coupled
35 to DLL output circuit 314 and generates output clock signal
36 O_CLK. Similarly, variable delay circuit 420 is coupled to

1 DFS output circuit 324 and generates frequency adjusted
2 clock signal FREQ_CLK.

3 In digital clock manager 400, DLL output delay 316 and
4 DFS output delay 326 can not be adequately matched.
5 However, variable delay circuit 410, which provides
6 additional delay to DLL output delay 316, and variable delay
7 circuit 420, which provides additional delay to DFS output
8 delay 326 can be used to synchronize output clock signal
9 O_CLK with frequency adjusted clock signal FREQ_CLK.
10 Specifically, DLL output delay 316 plus the delay provided
11 by variable delay circuit 410 should be matched with DFS
12 output delay 326 plus the delay provided by variable delay
13 circuit 420. In many embodiments of the present invention,
14 delay match can be achieved using only one of variable delay
15 circuits 410 or 420. Therefore, these embodiments would not
16 need to include both variable delay circuit 410 and variable
17 delay circuit 420.

18 Fig. 5 is a block diagram of a digital clock manager
19 500 in accordance with one embodiment of the present
20 invention. Because, digital clock manager 500 is similar to
21 digital clock manager 300, similar reference numerals are
22 used for similar elements. In addition, descriptions of the
23 repeated elements are omitted for brevity. Digital clock
24 manager 500 reduces the time required to generate frequency
25 adjusted clock signal FREQ_CLK as compared to digital clock
26 manager 300. As is well known in the art, delay lock loops
27 operate in a lock acquisition mode prior to generating a
28 stable output clock signal. Similarly, digital frequency
29 synthesizers operate in various frequency search phases
30 prior to generating a stable frequency adjusted clock
31 signal. In digital clock manager 300, delay lock loop 310
32 must first undergo a lock acquisition mode to generate
33 synchronizing clock signal SYNCH_CLK. Then digital
34 frequency synthesizer must undergo various frequency search
35 phases prior to generating frequency adjusted clock signal
36 FREQ_CLK.

1 However, in digital clock manager 500, lock acquisition
2 by delay lock loop 310 and frequency search phases by
3 digital frequency synthesizer 320 can occur simultaneously
4 to reduce the time necessary to generate output clock signal
5 O_CLK and frequency adjusted clock signal FREQ_CLK.
6 Specifically, digital clock manager 500 includes a
7 multiplexer 510, having a first input terminal coupled to
8 receive reference clock signal REF_CLK, a second input
9 terminal coupled to receive synchronizing clock signal
10 SYNCH_CLK and an output terminal coupled to digital
11 frequency synthesizer 320. Multiplexer 510 is controlled by
12 a clock transition control signal CLK_TRAN from digital
13 frequency synthesizer 320. Clock transition control signal
14 CLK_TRAN is driven to an inactive state while delay locked
15 loop is performing lock acquisition or digital frequency
16 synthesizer 320 is not ready for a clock transition. If
17 clock transition control signal is in the inactive state,
18 multiplexer 510 couples reference clock signal REF_CLK to
19 digital frequency synthesizer 320.

20 Because reference clock signal REF_CLK is already at
21 reference frequency F_REF, digital frequency synthesizer 320
22 can perform the required frequency search phases using
23 reference clock signal REF_CLK. After delay lock loop 310
24 finishes lock acquisition, a control signal DLL_LOCKED is
25 driven to an active state (e.g., logic high) signaling
26 digital frequency synthesizer 320 that delay lock loop 310
27 has completed lock acquisition. Then, when digital
28 frequency synthesizer is ready for transitioning to
29 synchronizing clock signal SYNCH_CLK, clock transition
30 control signal CLK_TRAN is driven to the active state, which
31 causes synchronizing clock signal SYNCH_CLK to be provided
32 to digital frequency synthesizer 320. For example, in some
33 embodiments of the present invention, digital frequency
34 synthesizer 320 completes a frequency search phase prior to
35 driving control signal CLK_TRAN to select synchronizing
36 clock signal SYNCH_CLK. Furthermore, in some embodiments of

1 the present invention, digital frequency synthesizer 320 is
2 halted prior to switching from reference clock signal
3 REF_CLK to synchronizing clock signal SYNCH_CLK and then
4 restarted. Thus, digital clock manager 500 reduces the time
5 required to generate frequency adjusted clock signal
6 FREQ_CLK by allowing acquisition lock by delay lock loop 310
7 and frequency searches by digital frequency synthesizer 320
8 to operate simultaneously.

9 Figure 6 is a block diagram of a system using a delay
10 lock loop 600 in accordance with one embodiment of the
11 present invention. Delay lock loop 600 comprises a delay
12 line 610, a clock phase shifter 650, a controller 630, an
13 output generator 640, and a phase detector 620. Delay lock
14 loop 600 receives reference clock signal REF_CLK on a
15 reference input terminal 602 and generates output clock
16 signal O_CLK on output terminal 604. As explained above
17 with respect to Figure 1, output clock signal O_CLK is
18 skewed by clock skew 180 into skewed clock signal S_CLK,
19 which clocks logic circuits 190. Skewed clock signal S_CLK
20 is also fed back to a feedback terminal 606 of delay lock
21 loop 600 on feedback path 170.

22 Within delay lock loop 600, reference clock signal
23 REF_CLK is delayed by delay line 610 to generate delayed
24 clock signal D_CLK. Delayed clock signal D_CLK is delayed
25 from clock signal REF_CLK by a propagation delay D in delay
26 line 610. One embodiment of delay lock loop 600 uses an
27 adjustable delay line described in U.S. Patent Application
28 Serial No. 09/102,704 (Attorney Docket No. X-440), entitled
29 "Glitchless Delay Line Using Gray Code Multiplexer" by
30 Andrew K. Percy, which is incorporated herein by reference.
31 However, other adjustable delay lines can also be used with
32 delay lock loop 600. Delayed clock signal D_CLK is provided
33 to an input terminal of a clock phase shifter 650 and to an
34 input terminal of an output generator 640. Delayed clock
35 signal D_CLK is also provided to digital frequency
36 synthesizer 320 as synchronizing clock signal SYNCH_CLK.

1 Clock phase shifter 650 generates one or more phase-
2 shifted clock signals P_CLK_1 to P_CLK_N-1, where N is a
3 positive integer. In one embodiment, phase-shifted clock
4 signal P_CLK_1 is phase-shifted by $360/N$ degrees from
5 delayed clock signal D_CLK. Phase-shifted clock signal
6 P_CLK_2 is phase-shifted by $2*(360/N)$ degrees. Phase-
7 shifted clock signal P_CLK_N-1 is phase-shifted by
8 $(N-1)*(360/N)$ degrees. Thus, in general a phase-shifted
9 clock signal P_CLK_Z is phase-shifted by $Z*(360/N)$, where Z
10 is an integer between 1 and (N-1), inclusive. Delayed clock
11 signal D_CLK can be considered a phase-shifted clock signal
12 P_CLK_0 since delayed clock signal D_CLK has a 0 degree
13 phase shift from itself. Further, in some embodiments of
14 delay lock loop 600, clock phase shifter 650 generates a
15 phase-shifted signal P_CLK_N that has the same phase and
16 frequency as delayed clock signal D_CLK.

17 Thus, in an embodiment of clock phase shifter 650 where
18 N is equal to four, phase-shifted clock signal P_CLK_1 is
19 phase-shifted 90 degrees from delayed clock signal D_CLK.
20 It logically follows that phase-shifted clock signal P_CLK_2
21 is phase-shifted by 180 degrees from delayed clock signal
22 D_CLK and phase-shifted clock signal P_CLK_3 is phase-
23 shifted by 270 degrees from delayed clock signal D_CLK.
24 However, the principles of the present invention are also
25 suitable for other embodiments of clock phase shifter 650
26 using other patterns of phase shifting between the phase-
27 shifted clock signals.

28 Phase shifting is a concept in the frequency domain of
29 a clock signal. The equivalent of phase shifting in the
30 time domain is delaying the clock signal. Specifically, if
31 a first clock signal is phase-shifted from a second clock
32 signal by X degrees, the first clock signal is delayed by
33 $X*(P/360)$, where P is the period of the first and second
34 clock signals. Thus, if phase-shifted clock signal P_CLK_1
35 is phase-shifted 90 degrees from delayed clock signal D_CLK,

1 phase-shifted clock signal P_CLK_1 is delayed by one-fourth
2 of the period of delayed clock signal D_CLK. To distinguish
3 delays caused by phase shifting from other propagation
4 delays, delays caused by phase shifting are referred to as
5 phase-shifted delays P_D_Z. Since a phase-shifted clock
6 signal P_CLK_Z is phase-shifted by $Z \cdot (360/N)$ degrees, phase-
7 shifted clock signal P_CLK_Z has a phase-shifted delay P_D_Z
8 equal to $Z \cdot (P/N)$, where Z is an integer between 1 and (N-1),
9 inclusive.

10 Figure 7 illustrates for a timing diagram for delay
11 lock loop 600 (Figure 6) wherein N equals 4. Specifically,
12 clock phase shifter 650 generates phase-shifted clock signal
13 P_CLK_1 90 degrees out of phase with delayed clock signal
14 D_CLK. Thus, phase-shifted clock signal P_CLK_1 is delayed
15 by one-fourth of clock period P. Clock phase shifter 650
16 generates phase-shifted clock signal P_CLK_2 180 degrees out
17 of phase with delayed clock signal D_CLK. Thus, phase-
18 shifted clock signal P_CLK_2 is delayed by half of clock
19 period P. Finally, clock phase shifter 650 generates phase-
20 shifted clock signal P_CLK_3 270 degrees out of phase with
21 delayed clock signal D_CLK. Thus, phase-shifted clock
22 signal P_CLK_3 is delayed by three-fourths of clock period
23 P.

24 Returning to Figure 6, clock phase shifter 650 provides
25 the phase-shifted clock signals to various input terminals
26 of output generator 640. In some embodiments of delay lock
27 loop 600, clock phase shifter 650 can be configured using
28 one or more configuration signals CFG on an optional
29 configuration bus 660. An embodiment of clock phase shifter
30 650 that is configured by configuration signals CFG is
31 described below with respect to Figure 10. Configuration
32 signals CFG are received on configuration terminals 608 and
33 are routed to clock phase shifter 650 and controller 630 by
34 configuration bus 660. Output generator 640 selects either
35 delayed clock signal D_CLK or one of the phase-shifted clock
36 signals to provide as output clock signal O_CLK as dictated

1 by controller 630 (described below). For embodiments of
2 delay lock loop 600 in which clock phase shifter 650
3 provides phase-shifted clock signal P_CLK_N, output
4 generator 640 can use phase-shifted clock signal P_CLK_N in
5 place of delayed clock signal D_CLK. Controller 630
6 controls output generator 640.

7 Controller 630 receives phase information regarding
8 reference clock signal REF_CLK and skewed clock signal S_CLK
9 from phase detector 620. Specifically, phase detector 620
10 informs controller 630 whether propagation delay D from
11 delay line 610 should be increased or decreased to achieve
12 synchronization of skewed clock signal S_CLK with reference
13 clock signal REF_CLK. For embodiments of phase detector 620
14 that only determine whether to increase or decrease
15 propagation delay D, a jitter filter (not shown) can be used
16 to reduce clock jitter. In one embodiment, the jitter
17 filter is an up/down counter (not shown) that decrements by
18 one if propagation delay D should be decreased and
19 increments by one if propagation delay D should be
20 increased. However, propagation delay D is not adjusted
21 until the up/down counter reaches 0 or some other
22 predetermined number. When propagation delay D is adjusted,
23 the up/down counter is reset to one-half the maximum value.
24 In other embodiments, phase detector 620 calculates the
25 amount propagation delay D should be increased or decreased.
26 During lock acquisition, controller 630 attempts to
27 synchronize skewed clock signal S_CLK with reference clock
28 signal REF_CLK so that initial propagation delay ID of
29 propagation delay D is within a lock window W.

30 Figure 8 illustrates the concepts of lock window W. As
31 explained above, propagation delay D must be between minimum
32 propagation delay D_MIN and maximum propagation delay D_MAX.
33 Typical values for D_MIN and D_MAX are 3.2 nanoseconds and
34 46.8 nanoseconds, respectively. During lock acquisition,
35 controller 630 ensures that initial propagation delay ID of
36 propagation delay D is within lock window W. Specifically,

1 when synchronization is first established initial
2 propagation delay ID must be between lock window minimum
3 W_MIN and lock window maximum W_MAX. The limits on lock
4 window W are set to guarantee that once delay lock loop 600
5 completes locks acquisition, delay lock loop 600 can
6 maintain synchronization as long as the system containing
7 delay lock loop 600 operates within the design guidelines of
8 the system.

9 For example, the system containing delay lock loop 600
10 generally can operate in a range of operating conditions.
11 The range of operating conditions includes a maximum extreme
12 condition in which propagation delay SKEW is maximized at a
13 propagation delay value SKEW_MAX. Similarly, the range of
14 operating conditions also includes a minimum extreme
15 condition in which propagation delay SKEW is minimized at a
16 propagation delay value SKEW_MIN. Thus, the maximum change
17 (DELTA_SKEW) in propagation delay SKEW during operation of
18 the system is equal to propagation delay value SKEW_MAX
19 minus propagation delay value SKEW_MIN (i.e., DELTA_SKEW =
20 SKEW_MAX - SKEW_MIN). For maximum protection during lock
21 maintenance, lock window minimum W_MIN can be equal to
22 minimum propagation delay D_MIN plus DELTA_SKEW. Similarly,
23 lock window maximum W_MAX can be equal to maximum
24 propagation delay D_MAX minus DELTA_SKEW. In one embodiment
25 of the present invention, lock window minimum W_MIN is equal
26 to approximately 16.5% of maximum propagation delay D_MAX
27 and lock window maximum W_MAX is equal to approximately
28 67.8% of maximum propagation delay D_MAX.

29 As explained above with respect to Figure 1, for a
30 conventional delay lock loop synchronization of skewed clock
31 signal S_CLK with reference clock signal REF_CLK is achieved
32 when propagation delay D plus propagation delay SKEW is
33 equal to a multiple of period P. In equation form:

$$D + SKEW = MULT(P) \quad (1)$$

1 where MULT(P) refers to a multiple of P. Usually, the
2 smallest multiple of P greater than SKEW is used.

3 With delay lock loop 600, controller 630 can also use
4 the delays from the phase-shifted clock signals. Thus delay
5 lock loop 600 can achieve synchronization if propagation
6 delay D plus a phase-shifted delay P_D from a phase-shifted
7 clock signal plus propagation delay SKEW is a multiple of
8 period P. In equation form:

$$9 \quad D + P_D_Z + SKEW = MULT(P) \quad (2)$$

10 where P_D_Z refers to a phase-shifted delay from phase-
11 shifted clock signal P_CLK_Z. Usually, the smallest
12 multiple of P greater than propagation delay SKEW plus
13 phase-shifted delay P_D_Z is used. As explained above with
14 respect to Figure 6, in one embodiment of clock phase
15 shifter 650 phase-shifted delay P_D_Z of a phase-shifted
16 clock signal P_CLK_Z is equal to $Z*(P/N)$, where Z is an
17 integer between 0 and (N-1), inclusive. If Z is equal to 0,
18 controller 630 causes output generator 640 to use delayed
19 clock signal D_CLK as output clock signal O_CLK. Thus,
20 phase-shifted delay P_D_0 is equal to 0.

21 For clarity, initial delay ID can be referred to
22 initial delay ID_0 if output generator 640 uses delayed
23 clock signal D_CLK for output clock signal O_CLK.
24 Similarly, initial delay ID can be referred to as initial
25 delay ID_Z, if output generator 640 uses phase-shifted clock
26 signal P_CLK_Z for output clock signal O_CLK, where Z is a
27 positive integer between 1 and (N-1), inclusive. Thus, at
28 the end of lock acquisition, equation (2) can be rewritten
29 as:

$$30 \quad ID_Z + P_D_Z + SKEW = MULT(P) \quad (3)$$

31 Re-arranging equation (3) provides:
32
33
34
35

$$ID_Z = MULT(P) - SKEW - P_D_Z \quad (4)$$

and substituting $Z*(P/N)$ for P_D_Z provides:

$$ID_Z = MULT(P) - SKEW - Z*(P/N) \quad (5)$$

Usually, the smallest multiple of P that results in a positive initial delay ID_Z is used. In situations where initial delay ID_Z is less than minimum propagation delay D_MIN or greater than maximum propagation delay D_MAX , delay lock loop 600 cannot synchronize skewed clock signal S_CLK with reference clock signal REF_CLK using phase-shifted clock signal P_CLK_Z .

Because controller 630 can select any one of phase-shifted clock signals P_CLK_Z to drive output clock signal O_CLK , controller 630 can select from N initial delay values. The possible initial delay values range from a minimum offset value $(MULT(P)-SKEW)$ to a maximum value $(MULT(P)-SKEW) \& (N-1)/N$ period P . The difference between each initial delay value is period P divided by N . For example, if N equals four, period P equals 40 nanoseconds, and propagation delay $SKEW$ equals 25 nanoseconds; then initial delays ID_0 , ID_1 , ID_2 , and ID_3 equal 15 nanoseconds, 5 nanoseconds, 35 nanoseconds, and 25 nanoseconds, respectively (as calculated using equation (5)). If N equals four, period P equals 40 nanoseconds, and propagation delay $SKEW$ equals 55 nanoseconds; then initial delays ID_0 , ID_1 , ID_2 , and ID_3 equal 25 nanoseconds, 15 nanoseconds, 5 nanoseconds, and 35 nanoseconds, respectively. Thus, controller 630 is likely to find one or more initial delay values within lock window W . If more than one initial delay value is within lock window W , controller 630 can select any one of the initial delay values within lock window W .

Some embodiments of controller 630 can perform the calculations described above to determine which phase-

1 shifted clock signal P_CLK_Z to use. However, other
2 embodiments use trial and error to determine which phase-
3 shifted clock signal P_CLK_Z to use. An embodiment of
4 controller 630 that uses trial and error is described below
5 with respect to Figure 12.

6 Figure 9 illustrates one embodiment of clock phase
7 shifter 650 of Figure 6. The embodiment of clock phase
8 shifter 650 in Figure 9 comprises a phase detector 920 and a
9 plurality of delay lines 910_1 to 910_N. Delay lines 910_1
10 to 910_N are coupled in series. The input terminal of delay
11 line 910_1 receives an input clock signal such as delayed
12 clock signal D_CLK (Figure 6). The output terminal of delay
13 line 910_N is coupled to an input terminal of phase detector
14 920. Phase detector 920 also receives input clock signal
15 D_CLK on another input terminal. Phase detector 920
16 controls all the delay lines in parallel via control line
17 925, and each delay line provides the same amount of
18 propagation delay. Consequently, input clock signal D_CLK
19 and the clock signal P_CLK-N on the output terminal of delay
20 line 910_N are synchronized, i.e., in phase. Further, phase
21 detector 920 causes the total propagation delay generated by
22 delay lines 910_1 to 910_N to be equal to one period P of
23 the input clock. Thus, each delay line provides a
24 propagation delay of P/N . Thus, the output terminal of
25 delay line 910_1 provides a clock signal that is delayed
26 from the input clock signal by P/N whereas the output
27 terminal of delay line 910_2 provides a clock signal that is
28 delayed from the input clock signal by $2 \cdot P/N$. In general,
29 the output terminal of delay line 910_Z provides a clock
30 signal that is delayed from the input clock signal by $Z \cdot P/N$,
31 where Z is an integer between 1 and N-1, inclusive.
32 Accordingly, if the input clock signal is delayed clock
33 signal D_CLK, the output terminals of delay lines 910_1 to
34 910_N-1 provide phase-shifted clock signals P_CLK_1 to
35 P_CLK_N-1, respectively. Some embodiments of clock phase
36 shifter 650 also generate a clock signal P_CLK_N on the

1 output terminal of delay line 910_N that has the same phase
2 as delayed clock signal D_CLK.

3 Figure 10 shows a configurable embodiment of clock
4 phase shifter 650 of Figure 6. Specifically, the clock
5 phase shifter of Figure 10 can be configured in a first mode
6 to produce three phase-shifted clock signals that are 90
7 degrees, 180 degrees, and 270 degrees out of phase with an
8 input clock signal. In a second mode, the clock phase
9 shifter of Figure 10 produces a single phase-shifted clock
10 signal that is 180 degrees out of phase with the input clock
11 signal. The clock phase shifter of Figure 10 comprises a
12 phase detector 1020, delay lines 1010_1, 1010_2, 1010_3, and
13 1010_4, and multiplexers 1030_1, 1030_2, 1030_3, and 1030_4.
14 A configuration line 1040 is coupled to the select terminal
15 of multiplexers 1030_1 to 1030_4.

16 The input terminal of delay line 1010_1 is coupled to
17 receive an input clock signal such as delayed clock signal
18 D_CLK (Figure 6). The output terminal of each delay line
19 1010_Z is coupled to the logic one input terminal of
20 multiplexer 1030_Z, where Z is an integer between 1 and 4,
21 inclusive. The output terminal of each multiplexer 1030_Z
22 is coupled to the input terminal of delay line 1010_Z+1,
23 where Z is an integer between 1 and 3, inclusive. The
24 output terminal of multiplexer 1030_4 is coupled to an input
25 terminal of phase detector 1020. The logic zero input
26 terminals of multiplexer 1030_1 and multiplexer 1030_3 are
27 coupled to ground. However, the logic zero input terminal
28 of multiplexer 1030_2 is coupled to the output terminal of
29 delay line 1010_1. Similarly, the logic zero input terminal
30 of multiplexer 1030_4 is coupled to the output terminal of
31 delay line 1010_3. Phase detector 1020 also receives input
32 clock signal D_CLK on another input terminal. Phase
33 detector 1020 controls delay lines 1010_1 to 1010_4 in
34 parallel as described above with respect to phase detector
35 920.

1 If configuration line 1040 is pulled to logic one,
2 which puts the embodiment of Figure 10 into the first mode,
3 delay lines 1010_1 to 1010_4 are coupled in series. In the
4 first mode, each delay line provides a delay of $P/4$. Thus,
5 if the input clock signal is delayed clock signal D_CLK, the
6 output terminal of each multiplexer 1030_Z can provide
7 phase-shifted clock signals P_CLK_1, P_CLK_2, and P_CLK_3.

8 However, if configuration line 1040 is pulled to logic
9 zero, which puts the embodiment of Figure 10 into the second
10 mode, only delay line 1010_1 and delay line 1010_3 are
11 coupled in series. Delay lines 1010_2 and 1010_4 have their
12 input terminal coupled to ground through multiplexers 1030_1
13 and 1030_3, respectively. In the second mode delay line
14 1010_1 and 1010_3 each provide a delay of $P/2$. Coupling the
15 input terminals of delay lines 1010_2 and 1010_4 to ground
16 reduces power consumption and switching noise. However, in
17 the second mode the embodiment of Figure 10 produces only
18 one output clock signal, which is 180 degrees out of phase
19 with the input clock signal and is generated at the output
20 terminal of multiplexer 1030_2.

21 Figure 11 shows one embodiment of output generator 640
22 of Figure 6. The output generator of Figure 11 comprises an
23 N-input multiplexer 1110. N-input multiplexer 1110 has N
24 input terminals, referenced as 1110_0 to 1110_N-1, select
25 terminals 1112, and an output terminal 1114. When the
26 embodiment of output generator 640 of Figure 11 is used in
27 delay lock loop 600 of Figure 6, select terminals 1112 are
28 coupled to controller 630, input terminal 1110_0 is coupled
29 to receive delayed clock signal D_CLK, output terminal 1114
30 provides output clock signal O_CLK, and input terminals
31 1110_1 to 1110_N-1 are coupled to receive phase-shifted
32 clock signals P_CLK_1 to P_CLK_N-1, respectively. Select
33 signals on select terminals 1112 determine which input
34 signal is provided on output terminal 1114. Other
35 embodiments of output generator 640 may include additional
36 circuitry, such as clock buffers and clock dividers. In

1 addition, some embodiments of output generator 640 drive
2 additional clock signals, such as various versions of the
3 phase-shifted clock signals.

4 Figure 12 shows a state diagram 1200 for one embodiment
5 of controller 630 of Figure 6. On power-up or reset,
6 controller 630 transitions to a reset stage 1210. In reset
7 stage 1210, controller 630 sets a phase counter (not shown)
8 to zero, which causes output generator 640 to provide
9 delayed clock signal D_CLK as output clock signal O_CLK, and
10 adjusts propagation delay D of delay line 610 (Figure 6) to
11 a starting delay value. Starting delay values for
12 propagation delay D include, for example, minimum
13 propagation delay D_MIN, maximum propagation delay D_MAX, or
14 the average of minimum propagation delay D_MIN and maximum
15 propagation delay D_MAX. Controller 1210 then transitions
16 to lock acquisition stage 1220.

17 In lock acquisition stage 1220, controller 630
18 synchronizes reference clock signal REF_CLK and skewed clock
19 signal S_CLK. Specifically, controller 630 adjusts
20 propagation delay D of delay line 610 based on signals from
21 phase detector 620. Phase detector 620 determines whether
22 propagation delay D must be increased or decreased to
23 synchronize skewed clock signal S_CLK with reference clock
24 signal REF_CLK. Lock acquisition is described above in
25 greater detail with respect to Figures 6-9; therefore, the
26 description is not repeated. In some embodiments, clock
27 phase shifter 650 is also reset by the power-on/reset
28 signal. For some of these embodiments, controller 630 does
29 not adjust propagation delay D until after clock phase
30 shifter 650 produces phase-shifted clock signals P_CLK_1 to
31 P_CLK_N-1. If controller 630 cannot synchronize skewed
32 clock signal S_CLK with reference clock signal REF_CLK,
33 controller 630 transitions to increment phase stage 1250,
34 described below. Otherwise, controller 630 transitions to
35 check lock window stage 1230 after controller 630
36 synchronizes skewed clock signal S_CLK with reference clock

1 signal REF_CLK (with an initial propagation delay ID in
2 delay line 610).

3 In check lock window stage 1230, controller 630 must
4 determine whether initial propagation delay ID is within
5 lock window W. Specifically, propagation delay ID is within
6 lock window W if propagation delay ID is greater than lock
7 window minimum W_MIN and less than lock window maximum
8 W_MAX. If initial propagation delay ID is not within lock
9 window W, controller 630 transitions to increment phase
10 stage 1250. Otherwise, controller 630 transitions to lock
11 maintenance stage 1240.

12 In lock maintenance stage 1240, controller 630 adjust
13 propagation delay D of delay line 610 to maintain
14 synchronization of skewed clock signal S_CLK with reference
15 clock signal REF_CLK. Lock maintenance is described above
16 in greater detail; therefore, the description is not
17 repeated. As described above, the present invention can
18 maintain lock throughout the systems environment conditions.
19 Therefore, controller 630 remains in lock maintenance stage
20 1240 unless a reset occurs that causes controller 630 to
21 transition to reset stage 1210.

22 In increment phase stage 1250, controller 630
23 increments the phase counter, which causes output generator
24 640 to select a different phase-shifted clock signal.
25 Further, controller 630 resets delay line 610 so that
26 propagation delay D returns to the starting delay value used
27 in reset stage 1210. Controller 630 then transitions to
28 lock acquisition stage 1220 and proceeds as described above.

29 Figure 13 is a block diagram of another embodiment of
30 delay lock loop 600. The embodiment of Figure 13 uses the
31 same principles as described above with respect to the
32 embodiment of Figure 6. However, in the embodiment of
33 Figure 13, clock phase shifter 650 generates phase-shifted
34 clock signals P_CLK_1 to P_CLK_N-1 using reference clock
35 signal REF_CLK. Reference clock signal REF_CLK and phase-
36 shifted clock signals P_CLK_1 to P_CLK_N-1 are coupled to an

1 input selector 1340. Input selector 1340 selects either
2 reference clock signal REF_CLK or one of phase-shifted clock
3 signals P_CLK_1 to P_CLK_N-1 as a delay line input clock
4 signal DLI_CLK, which is provided to the input terminal of
5 delay line 610. Delay line 610 drives output clock signal
6 O_CLK. A controller 1330 controls input selector 1340 and
7 delay line 610 based on the phase information provided by
8 phase detector 620 so that delay line 610 provides a
9 propagation delay D that synchronizes skewed clock signal
10 S_CLK with reference clock signal REF_CLK. Input selector
11 1340 can be implemented using the same circuit design as
12 output generator 640.

13 Fig. 14(a) is a block diagram of a digital frequency
14 synthesizer 1400 in accordance with one embodiment of the
15 present invention. Digital frequency synthesizer 1400
16 generates a frequency adjusted clock signal FREQ_CLK having
17 a clock frequency F_ADJ equal to a clock frequency F_SYNCH
18 of a synchronizing clock signal SYNCH_CLK multiplied by a
19 multiplier M and divided by a divider D (i.e.,
20 $F_{ADJ} = M \cdot F_{SYNCH} / D$). As explained above, when digital
21 frequency synthesizer 320 is used with digital clock manager
22 300, 400, or 500, clock frequency F_SYNCH of synchronizing
23 clock signal SYNCH_CLK is equal to clock frequency F_REF of
24 reference clock signal REF_CLK. Digital frequency
25 synthesizer 1400 comprises clock dividers 1410 and 1420,
26 optional clock selector 1430, phase comparator 1440,
27 halt/restart circuit 1445, initialization circuit 1450,
28 oscillator control circuit 1460, and variable digital
29 oscillator 1470. Clock divider 1410 receives frequency
30 adjusted clock signal FREQ_CLK, which is generated by
31 variable digital oscillator 1470, and generates feedback
32 clock signal FBK_CLK having a frequency F_FBK equal to
33 frequency F_ADJ of output clock FREQ_CLK divided by
34 multiplier M. Clock divider 1410 drives feedback clock
35 signal FBK_CLK to initialization circuit 1450 and phase
36 comparator 1440. Clock divider 1420 receives synchronizing

1 clock signal SYNCH_CLK and generates divided synchronizing
2 clock signal D_SYNCH_CLK having a frequency F_{D_SYNCH} equal
3 to frequency F_{SYNCH} of synchronizing clock signal SYNCH_CLK
4 divided by divider D. Clock divider 1420 drives divided
5 synchronizing clock signal D_SYNCH_CLK to initialization
6 circuit 1450 and phase comparator 1440.

7 Clock selector 1430 receives both synchronizing clock
8 signal SYNCH_CLK and frequency adjusted clock signal
9 $FREQ_CLK$ and selectively drives either synchronizing clock
10 signal SYNCH_CLK or frequency adjusted clock signal $FREQ_CLK$
11 as control clock signal CTRL_CLK to initialization circuit
12 1450 and oscillator control circuit 1460. Generally,
13 synchronizing clock signal SYNCH_CLK is used during a coarse
14 frequency search phase. Then, frequency adjusted clock
15 signal $FREQ_CLK$ is used for a fine frequency search phase as
16 well as during a clock maintenance phase, i.e., maintaining
17 the frequency of frequency adjusted clock signal $FREQ_CLK$ at
18 the selected frequency. The coarse frequency search phase,
19 the fine frequency search phase, and the maintenance phase
20 for one embodiment of the present invention is described in
21 detail below. Halt/restart circuit 1445, which is used
22 during coarse frequency search phase and the fine frequency
23 search phase, is described below.

24 At power-on or reset, initialization circuit 1450
25 controls oscillator control circuit 1460 to tune variable
26 digital oscillator 1470 to generate frequency adjusted clock
27 signal $FREQ_CLK$. Specifically, initialization circuit 1450
28 tunes variable digital oscillator 1470 so that frequency
29 F_{ADJ} of frequency adjusted clock signal $FREQ_CLK$ is equal
30 to a selected frequency F_{SEL} , which equals frequency
31 F_{SYNCH} of synchronizing clock signal SYNCH_CLK multiplied
32 by multiplier M and divided by divider D. After frequency
33 F_{ADJ} of frequency adjusted clock signal $FREQ_CLK$ reaches
34 selected clock frequency F_{SEL} , initialization circuit 1450
35 passes control of oscillator control circuit 1460 and
36 variable digital oscillator 1470 to phase comparator 1440.

1 Phase comparator 1440 tunes variable digital oscillator 1470
2 to maintain frequency F_{ADJ} at selected frequency F_{SEL}
3 despite environmental changes such as temperature.

4 Some embodiments of digital frequency synthesizer 1400
5 can use conventional clock dividers, clock selectors,
6 halt/restart circuits, and phase comparators. However,
7 detailed descriptions of specific embodiments of
8 initialization circuits 1450, oscillator control circuit
9 1460, and variable digital oscillator 1470 are described
10 below.

11 Fig. 14(b) is a timing diagram for digital frequency
12 synthesizer 1400. For clarity, Fig 14(b) is idealized and
13 omit such factors as propagation delay and skewing. In Fig.
14 14(b), multiplier M is equal to 7 and divider D is equal to
15 5. Thus, as shown in Fig. 14(b), divided synchronizing
16 clock signal D_SYNCH_CLK has a rising edge, such as rising
17 edges 1421, 1423, and 1425, at every fifth rising edge of
18 synchronizing clock signal $SYNCH_CLK$, i.e., at rising edges
19 1401, 1403, and 1405. Similarly, feedback clock signal
20 FBK_CLK has a rising edge, such as rising edges 1411, 1413,
21 and 1415, every seventh rising edge of frequency adjusted
22 clock signal $FREQ_CLK$, i.e., at rising edges 1471, 1473 and
23 1475. When frequency F_{ADJ} of frequency adjusted clock
24 signal $FREQ_CLK$ is equal to selected frequency F_{SEL} and
25 synchronizing clock signal $SYNCH_CLK$ is in phase with
26 frequency adjusted clock signal $FREQ_CLK$, feedback clock
27 signal FBK_CLK and divided synchronizing clock signal
28 D_SYNCH_CLK have the same phase and frequency. Accordingly,
29 initialization circuit 1450 and phase comparator 1440 tune
30 variable digital oscillator 1470 to match the phase and
31 frequency of divided synchronizing clock signal D_SYNCH_CLK
32 and feedback clock signal FBK_CLK to drive frequency
33 adjusted clock signal $FREQ_CLK$ at selected frequency F_{SEL} .
34 When the phase and frequency of divided synchronizing clock
35 signal D_SYNCH_CLK and feedback clock signal $FBCK_CLK$ match,
36 every M th rising edge of frequency adjusted clock signal

1 FREQ_CLK aligns with a rising edge of synchronizing clock
2 signal SYNCH_CLK. For example, rising edges 1471 and 1473
3 of frequency adjusted clock signal FREQ_CLK align with
4 rising edges 1401 and 1403 of synchronizing clock signal
5 SYNCH_CLK. The alignments are commonly referred to as
6 concurrences. The time between two consecutive concurrences
7 is commonly referred to as a concurrence period.

8 Fig. 15 is a block diagram of an embodiment of variable
9 digital oscillator 1470. The embodiment of Fig.3 comprises
10 a dual-input edge-triggered SR circuit 1510, an inverter
11 1540, and a variable delay line 1520 having a low precision
12 delay line 1525 and a trim circuit 1527. Dual-input edge-
13 triggered SR circuit 1510 includes a first set input
14 terminal S_IN1, a first set enable input terminal S_EN1, a
15 second set input terminal S_IN2, a second set enable input
16 S_EN2, a first reset input terminal R_IN1, a first reset
17 enable input terminal R_EN1, a second reset input terminal
18 R_IN2, a second reset enable input terminal R_EN2, and an
19 output terminal OUT. Operation and construction of dual-
20 input edge-triggered SR circuits are well known in the art
21 and therefore are not described in detail herein. Table 1
22 provides a truth table for an active high version of dual-
23 input edge-triggered SR CIRCUIT 1510. Basically, an active
24 (e.g., rising) edge of a set input signal on a set terminal
25 while the corresponding set enable signal at the set enable
26 terminal is at an enabled logic level (e.g., logic high)
27 causes output terminal OUT to drive an output signal to an
28 active state (e.g., logic high). Conversely, an active
29 (e.g., rising) edge on a reset input signal on a reset
30 terminal while the corresponding reset enable signal on the
31 corresponding reset enable terminal is at an enabled logic
32 level (e.g., logic high) causes output terminal OUT to drive
33 an output signal to an inactive state (e.g., logic low).
34 For clarity, the circuits herein are described using logic
35 high as the enabled logic level and the active logic level.
36 Similarly, rising edges are used as the active edges.

However, those skilled in the art can apply the principles of the present invention using different enabled logic levels, active logic levels, and active edges.

TABLE 1

S_IN1	S_EN1	S_IN2	S_EN2	R_IN1	R_EN1	OUT
RE	H	X	X	X	X	H
X	X	RE	H	X	X	H
X	X	X	X	RE	H	L

where RE is a rising edge, H is logic high, L is logic low, and X is a do not care condition.

Synchronizing clock signal SYNCH_CLK is coupled to first set input terminal S_IN1 and a reference clock enable signal R_CLK_EN is coupled to first enable input terminal S_EN1. Output terminal OUT of dual edge-triggered SR CIRCUIT 1510 drives frequency adjusted clock signal FREQ_CLK and is coupled to variable delay line 1520. In the embodiment of Fig. 15, variable delay line 1520 is implemented using a low precision delay line 1525 have a base delay BD and a trim circuit 1527 that provides a delay of 0, 0.25, 0.50, or 0.75 times base delay BD. Other embodiments of the present invention can use conventional variable delay lines. Variable delay line 1520 delays the output signal of dual-input edge-triggered SR circuit 1510 by a variable amount under the control of oscillator control circuit 1460 to generate delayed output signal D_OUT. Delayed output signal D_OUT is coupled to first reset input signal R_IN1 as well as the input terminal of inverter 1540. The output terminal of inverter 1540 is coupled to second set input terminal S_IN2. An oscillator enable signal OSC_EN is coupled to second set enable terminal S_EN2. Under normal operations, oscillator enable signal OSC_EN is in the logic high state to enable variable digital oscillator 1470. Therefore, a rising edge from output terminal OUT that is delayed by variable delay line 1520 causes dual-input edge-triggered SR circuit 1510 to transition to logic low. Conversely, a falling edge from

1 output terminal OUT that is delayed by variable delay line
2 1520 and inverted by inverter 1540 causes dual-input edge-
3 triggered SR circuit 1510 to transition to logic high.
4 Thus, variable digital oscillator 1470 generates a clock
5 signal such as frequency adjusted clock signal FREQ_CLK.
6 The frequency of frequency adjusted clock signal FREQ_CLK is
7 controlled by the amount of delay provided by variable delay
8 line 1520.

9 In the embodiment of Fig. 15, low precision variable
10 delay line 1525 provides a variable delay ranging from 0 to
11 127 times low precision base delay LBD, where low precision
12 base delay LBD is the smallest non-zero delay provided by
13 low precision variable delay 1525. Furthermore, trim
14 circuit 1530 provides an additional delay of 0, 0.25, 0.5 or
15 0.75 base delay units. Thus, in the embodiment of Fig. 15,
16 variable delay line 1520 can provide 512 delay values
17 ranging from 0 to 127.75 low precision base delay LBD in
18 multiples of 0.25 low precision base delay LBD. Thus, in
19 the embodiment of Fig. 15, variable delay line 1520 provides
20 a delay between 0 and 511 times a base delay BD, which is
21 equal to 0.25 times low precision base delay LBD.

22 Depending on the frequency F_SYNCH of synchronizing
23 clock signal SYNCH_CLK, multiplier M, and divisor D,
24 variable delay line 1520 may not be able to provide the
25 exact amount of delay necessary to generate frequency
26 adjusted clock signal FREQ_CLK at selected frequency F_SEL.
27 Fig. 16 illustrates this problem of using digital delay
28 lines in clock generation circuits. Specifically, Fig. 16
29 shows a synchronizing clock signal SYNCH_CLK, a conventional
30 frequency adjusted clock signal C_FREQ_CLK, and an frequency
31 adjusted clock signal FREQ_CLK generated using a dual-input
32 edge-triggered SR circuit 1510 in accordance with one
33 embodiment of the present invention. In Fig. 16, rising
34 edges 1651, 1661, and 1671 of synchronizing clock signal
35 SYNCH_CLK, conventional frequency adjusted clock signal

1 C_FREQ_CLK, and frequency adjusted clock signal FREQ_CLK,
2 respectively, are synchronized.

3 In Fig. 16, multiplier M is equal to 4 and divider D is
4 equal to 1. Synchronizing clock signal SYNCH_CLK has a
5 period of 50 nanoseconds. Accordingly, 25 nanoseconds
6 separates each consecutive clock edge in synchronizing clock
7 signal SYNCH_CLK. Ideally, variable delay line 1520 would
8 provide a delay of 6.25 nanoseconds, which is equal to 25
9 divided by 4. However, if the base delay unit of variable
10 delay line 1520 (Fig. 15) is one nanosecond, then variable
11 delay line 1520 is configured to provide 6 nanoseconds of
12 delay between consecutive edges of frequency adjusted clock
13 signal FREQ_CLK1. As explained above, during concurrence,
14 i.e., every 4 periods, the rising edge of conventional
15 frequency adjusted clock signal C_FREQ_CLK should occur at
16 the same time as the rising edge of synchronizing clock
17 signal SYNCH_CLK. However, as illustrated in Fig. 16,
18 rising edge 1665 of conventional output clock C_FREQ_CLK
19 precedes rising edge 1655 of synchronizing clock signal
20 SYNCH_CLK by 2 nanoseconds. The two nanosecond misalignment
21 reoccurs every concurrence period. Thus, over time the
22 misalignment can cause serious synchronization problems in
23 digital systems.

24 To eliminate the misalignment, just prior to
25 concurrence, i.e., when a rising edge of synchronizing clock
26 signal SYNCH_CLK should be aligned with a rising edge of
27 frequency adjusted clock signal FREQ_CLK, oscillator enable
28 signal OSC_EN is deasserted and reference clock enable
29 signal is asserted. Thus, during a concurrence the rising
30 edge of synchronizing clock signal SYNCH_CLK on input
31 terminal S_IN1 of dual-input edge-triggered SR circuit 1510
32 causes a rising edge on output terminal OUT of dual-input
33 edge-triggered SR circuit 1510, which drives frequency
34 adjusted clock signal FREQ_CLK. After concurrence,
35 oscillator enable signal OSC_EN is reasserted and reference
36 clock enable signal R_CLK_EN is deasserted. Thus, every Mth

1 clock period of frequency adjusted clock signal `FREQ_CLK`,
2 frequency adjusted clock signal `FREQ_CLK` is realigned with
3 synchronizing clock signal `SYNCH_CLK` even if variable delay
4 line 1520 does not provide the exact delay necessary to
5 drive frequency adjusted clock signal `FREQ_CLK` at selected
6 frequency `F_SEL`.

7 Accordingly, as shown in Fig. 16, rising edge 1675 of
8 frequency adjusted clock signal `FREQ_CLK` is aligned with
9 rising edge 1655 of synchronizing clock signal `SYNCH_CLK`.
10 Therefore, the time between falling edge 1671 of frequency
11 adjusted clock signal `FREQ_CLK` and rising edge 1675 of
12 frequency adjusted clock signal `FREQ_CLK` is 8 nanoseconds
13 rather than 6 nanoseconds. Thus, the time period during a
14 concurrence cycle of frequency adjusted clock signal
15 `FREQ_CLK` is equal to 50 nanoseconds rather than 48
16 nanoseconds as would be dictated by using only variable
17 delay line 1520 to control the clock edges of frequency
18 adjusted clock signal `FREQ_CLK`. Consequently, the average
19 frequency of frequency adjusted clock signal `FREQ_CLK` over
20 an concurrence period is equal to selected frequency `F_SEL`.

21 Fig. 17 is a block diagram of oscillator control
22 circuit 1460 in accordance with one embodiment of the
23 present invention. The embodiment of Fig. 17 includes a
24 delay line register 1710, an optional incrementer 1730, an
25 optional delay line fine tuning controller 1720, and an
26 optional OR gate 1740. Delay line register 1710 receives a
27 delay value `DV[8:0]` from initialization circuit 1450 (Fig.
28 14). The contents of delay line register 1710 are provided
29 to incrementer 1730 and initialization circuit 1450 as delay
30 value feedback signals `DV_FB[8:0]`. Initialization circuit
31 1450 adjusts delay value `DV[8:0]` during the coarse frequency
32 search phase to match frequency `F_ADJ` of frequency adjusted
33 clock signal `FREQ_CLK` with selected frequency `F_SEL` as
34 described below. Delay line register 1710 also receives a
35 carry signal `CARRY` and a borrow signal `BORROW` from delay
36 line fine tuning controller 1720. IF delay line fine tuning

1 controller 1720 is enabled, delay line register 1710 is
2 configured to increment when carry signal CARRY is in the
3 active logic level (e.g., logic high) and to decrement on
4 when borrow signal BORROW is in the active logic level
5 (e.g., logic high). Generation of carry signal CARRY and
6 borrow signal BORROW is described below.

7 The delay value in delay line register 1710 is
8 selectively incremented by incrementer 1730 to generate
9 delay select signals DELAY_SEL[8:0], which are coupled to
10 variable delay line 1520 (Fig. 15). Specifically, delay
11 line fine tuning controller 1720 drives a fine tuning
12 increment control signal FT_INC to incrementer 1730. If
13 fine tuning increment control signal FT_INC is at an active
14 logic level (e.g., logic high), then incrementer 1730
15 increments the value from delay line register 1710. Delay
16 line fine tuning controller 1720 is controlled by frequency
17 comparator 1450 using control signal A/!S or by phase
18 comparator 1440 (Fig. 14(a)) using phase comparator control
19 signal PC_CTRL. For the embodiment of Fig. 17, if delay
20 line fine tuning controller 1720 is enabled then if either
21 control signal A/!S or phase comparator signal PC_CTRL is in
22 the active state (i.e., logic high) then delay line fine
23 tuning controller 1720 is configured to add additional delay
24 during a concurrence period. Thus, OR gate 1740 generates
25 add delay signal ADD_DELAY from control signal A/!S and
26 phase comparator control signal PC_CTRL. The use of delay
27 line fine tuning controller 1720 is described in detail
28 below.

29 Fig. 18 is a block diagram of initialization circuit
30 1450 in accordance with one embodiment of the present
31 invention. Initialization circuit 1450 performs a coarse
32 frequency search to set the value in variable delay line
33 1520. Specifically, during the coarse frequency search
34 phase, the embodiment of Fig. 18 performs a fast binary
35 search to determine delay value DV[8:0] for delay line
36 register 1710, which causes frequency F_FBK of feedback

1 clock FBK_CLK and frequency F_D_SYNCH of divided reference
2 clock D_SYNCH_CLK to be equal. Other embodiments of
3 initialization circuit 1450 may use other methods to select
4 delay value DV[8:0] for delay line register 1710. The
5 embodiment of Fig. 18 comprises a right shift register 1830,
6 an adder/subtractor 1840, a frequency comparator 1850, and
7 an overflow register 1860.

8 Initially, adder/subtractor 1840 is configured to
9 provide a delay value DV[8:0] that causes variable delay
10 line 1520 to provide 50% of the maximum delay that can be
11 provided by variable delay line 1520. For the embodiment of
12 Fig. 15, delay value DV[8:0] is initially set at 256, i.e.,
13 halfway between 0 and 511. Right shift register 1830 is
14 initially configured to be equal to half of the initial
15 value of delay value DV[8:0]. Thus, for the embodiment of
16 Fig. 15, right shifter 1830 is configured with an initial
17 value of 128. Adder/subtractor 1840 is controlled by
18 frequency comparator 1850 to either add the value in right
19 shifter 1830 to the value in delay line register 1710 (Fig.
20 17) or to subtract the value in right shifter 1830 to the
21 value in delay line register 1710. Specifically, the value
22 in delay line register 1710 is provided by delay value
23 feedback signals DV_FB[8:0]. After each addition or
24 subtraction operation, the content of right shifter 1830 is
25 "right shifted", which effectively divides the value in
26 right shifter 1830 in half. However, right shifter 1830
27 maintains a minimum value of 1.

28 Frequency comparator 1850 receives feedback clock
29 signal FBK_CLK and divided reference signal D_SYNCH_CLK and
30 generates a control signal A/!S which dictates whether
31 adder/subtractor 1840 performs an ADD operation or a
32 SUBTRACT operation. Specifically, if frequency F_FBK of
33 feedback clock signal FBK_CLK is greater than frequency
34 F_D_SYNCH of divided synchronizing clock signal D_SYNCH_CLK,
35 the delay provided by variable delay line should be
36 increased. Accordingly, frequency comparator 1850 causes

1 adder/subtractor 1840 to perform an ADD operation by driving
2 control signal A/!S to the add logic level (typically logic
3 high). Conversely, if frequency F_FBK of feedback clock
4 signal FBK_CLK is less than frequency F_D_SYNCH of divided
5 synchronizing clock signal D_SYNCH_CLK, the delay provided
6 by variable delay line should be decreased. Accordingly,
7 frequency comparator 1850 causes adder/subtractor 1840 to
8 perform a SUBTRACT operation by driving control signal A/!S
9 to the subtract logic level (typically logic low). After
10 each addition or subtraction, halt/restart circuit 1445
11 (Fig. 14) halts and restarts initialization circuit 1450,
12 and oscillator control circuit 1460 so that frequency
13 adjusted clock signal FREQ_CLK is started in phase with
14 synchronizing clock signal SYNCH_CLK. Halting and
15 restarting allows frequency comparator 1850 to determine the
16 proper value of control signal A/!S without having to
17 compensate for phase variations. However, some embodiments
18 of the present invention may use frequency comparators that
19 automatically compensate for phase variations. For these
20 embodiments, halting and restarting may not be necessary.

21 In some embodiments of the present invention, frequency
22 comparator 1850 also generates a frequency comparator
23 reversal signal FC_REV. Frequency comparator reversal
24 signal FC_REV is driven to a active state (e.g., logic high)
25 when frequency F_FBK of feedback clock signal FBK_CLK
26 becomes greater than frequency F_D_SYNCH of divided
27 synchronizing clock signal D_SYNCH_CLK and also when
28 frequency F_D_SYNCH of divided synchronizing clock signal
29 D_SYNCH_CLK becomes greater than frequency F_FBK of feedback
30 clock signal FBK_CLK. In one embodiment of the present
31 invention, a coarse frequency search phase ends when the
32 value of right shifter 1830 is equal to one.

33 Table 2 provides an example of the operation for the
34 embodiment of initialization circuit 1450 in Fig. 18. In
35 the example of Table 2, a delay value DV of 371.5 provides
36 the optimum delay for matching frequency F_FBK of feedback

clock signal FBK_CLK to frequency F_D_SYNCH of divided synchronizing clock signal D_SYNCH_CLK.

TABLE 2

Coarse Frequency Search Step	Right Shifter 1830	Delay Line Register 1730	A/!S
0	128	256	1
1	64	384	0
2	32	320	1
3	16	352	1
4	8	368	1
5	4	376	0
6	2	372	0
7	1	370	1
8	1	371	1
9	1	372	0
10	1	371	1

As explained above initially delay line register 1710 is configured to contain 256 and right shift register 1830 is configured to contain 128. Because the ideal value for delay value DV is 371.5, control signal A/!S is in the Add state (i.e., logic high). At step 1, adder/subtractor 1840 adds 128 to 256; delay line register 1710 stores 384 (i.e., 256+128); and right shifter 1830 right shifts 128, which becomes 64. When delay line register 1710 contains 384 frequency comparator 1850 drives control line A/!S to the subtract logic level (i.e., logic low). Then, in step 2, adder/subtractor 1840 subtracts 64 from 384; delay line register 1710 stores 320 (i.e., 384-64); and right shifter 1830 right shifts 64 which becomes 32. When delay line register 1710 contains 320 frequency comparator 1850 drives control line A/!S to the add logic level (i.e., logic high). This process continues until the value in delay line register 1710 is as close to the optimum value as possible.

Overflow register 1860 receives output bit 9 of adder/subtractor 1840. If output bit 9 is active, an overflow conditions has occurred and must be remedied by an outside control system (not shown). Typically, overflow

conditions only occur if clock divider/multiplier 1400 is used with clock frequencies that are too fast or too slow compared to the possible delay time provided by variable delay line 1520.

As stated above, some embodiments of the present invention perform a fine frequency search using delay line fine tuning controller 1720 after initialization circuit 1450 establishes a delay value DV[8:0]. As explained above, variable digital delay lines may not be able to provide the exact delay necessary to generate frequency adjusted clock signal FREQ_CLK at selected frequency F_SEL. The present invention solves this problem by using dual-input edge-triggered SR circuit 1510 (Fig. 15) to synchronize rising clock edges on frequency adjusted clock signal FREQ_CLK to reference clock SYNCH_CLK during a concurrence of frequency adjusted clock signal FREQ_CLK and synchronizing clock signal SYNCH_CLK. As explained above, a concurrence occurs when a rising edge of frequency adjusted clock signal FREQ_CLK is suppose to be aligned with a rising edge synchronizing clock signal SYNCH_CLK, i.e., every Mth rising edge. However, between concurrence the frequency and phase of frequency adjusted clock signal FREQ_CLK may differ from an ideal clock signal at selected frequency F_SEL. Delay line fine tuning controller 1720 selectively adjusts the delay provided by variable delay line 1520 to better match the frequency and phase of the ideal frequency adjusted clock signal.

Effectively, delay line fine tuning controller 1720 adds additional precision to variable delay line 1520 by selectively increasing the delay provided by variable delay line 1520 by one base delay BD at various times during a concurrence period. Fig. 19 illustrates the advantages provided by delay line fine tuning controller 1720. Specifically, Fig. 19 shows a synchronizing clock signal SYNCH_CLK, an ideal frequency adjusted clock signal I_FREQ_CLK, an frequency adjusted clock signal FREQ_CLK1

1 using a dual-input edge-triggered SR circuit in accordance
2 with one embodiment of the present invention, and an
3 frequency adjusted clock signal `FREQ_CLK2` using both a dual-
4 input edge-triggered SR circuit and delay line fine tuning
5 controller 1720 in accordance with another embodiment of the
6 present invention.

7 In Fig. 19, multiplier M is equal to 4 and divider D is
8 equal to 1. Synchronizing clock signal `SYNCH_CLK` has a
9 period of 50 nanoseconds. Accordingly, 25 nanoseconds
10 separates each consecutive clock edge in synchronizing clock
11 signal `SYNCH_CLK`. Ideal frequency adjusted clock signal
12 `I_FREQ_CLK` has a period of 12.5 nanoseconds. Accordingly,
13 6.25 nanoseconds separates each consecutive clock edge in
14 ideal frequency adjusted clock signal `I_FREQ_CLK`. If the
15 base delay unit of variable delay line 1520 (Fig. 15) is one
16 nanosecond, then variable delay line 1520 is configured to
17 provide 6 nanoseconds of delay between consecutive edges of
18 frequency adjusted clock signal `FREQ_CLK1`. However, during
19 a concurrence, the rising edge of frequency adjusted clock
20 signal `FREQ_CLK1` is controlled by the rising edge of
21 synchronizing clock signal `SYNCH_CLK`. Accordingly, rising
22 edge 1935 of frequency adjusted clock signal `FREQ_CLK1` is
23 aligned with rising edge 1915 of synchronizing clock signal
24 `SYNCH_CLK`. Therefore, the time between falling edge 1934 of
25 frequency adjusted clock signal `FREQ_CLK1` and rising edge
26 1935 of frequency adjusted clock signal `FREQ_CLK1` is 8
27 nanoseconds. Thus, the average period during a concurrence
28 cycle of frequency adjusted clock signal `FREQ_CLK1` is equal
29 to 12.5 nanoseconds. However, frequency adjusted clock
30 signal `FREQ_CLK1` is distorted from ideal frequency adjusted
31 clock signal `I_FREQ_CLK` because the required extra delay
32 during a concurrence period is bunched at the end of the
33 concurrence period.

34 Delay line fine tuning controller 1720 selectively
35 increments the delay provided by delay line 1520 to more
36 closely match ideal frequency adjusted clock signal

1 I_FREQ_CLK. Rather than lumping the extra delay required to
2 match the average period of frequency adjusted clock signal
3 FREQ_CLK2 with ideal frequency adjusted clock signal
4 I_FREQ_CLK at the of the concurrence period, delay line fine
5 tuning controller 1720 spreads the additional required base
6 delay units over the entire concurrence period. Thus,
7 falling clock edge 1942 and rising clock edge 1943 of
8 frequency adjusted clock signal FREQ_CLK2 are separated by 7
9 nanoseconds rather than 6 nanoseconds. Similarly, falling
10 clock edge 2046 and rising clock edge 1947 of frequency
11 adjusted clock signal FREQ_CLK2 are separated by 7
12 nanoseconds rather than 6 nanoseconds. Thus, the waveform
13 of frequency adjusted clock signal FREQ_CLK2 more closely
14 matches ideal frequency adjusted clock signal I_FREQ_CLK
15 than frequency adjusted clock signal FREQ_CLK1.

16 Fig. 20 is a block diagram of a delay line fine tuning
17 controller 1720 in accordance with one embodiment of the
18 present invention. The embodiment of Fig. 20 includes an
19 up/down counter 2020, a modulo-M delta sigma circuit 2030,
20 AND gate 2040, an AND gate 2050, and an inverter 2060.
21 Up/down counter 2020 is configured to count in modulo M.
22 For example, if M is equal to 4, up/down counter 2020 would
23 count up in the sequence 0, 1, 2, 3, 0, 1, etc. and count
24 down in the sequence 3, 2, 1, 0, 3, 2, etc.

25 Conceptually, up/down counter 2020 is used to provide
26 high precision bits for delay line register 1710.
27 Specifically, the value in up/down counter 2020 indicates
28 the number of additional base delay units needed during a
29 concurrence period to more precisely match frequency F_ADJ
30 of frequency adjusted clock signal FREQ_CLK to selected
31 frequency F_SEL. In the example of Fig. 19, the base delay
32 value is 1 nanoseconds,
33 the delay value in delay line register 1710 is equal to 6
34 (i.e., one period of frequency adjusted clock signal
35 FREQ_CLK is 12 nanoseconds), the period of concurrence is 50
36 nanoseconds, and M is equal to 4. Thus, M periods of

1 frequency adjusted clock signal `FREQ_CLK` is equal to 48
2 nanoseconds (i.e., $4 * 12$ nanoseconds). However, since the
3 concurrence period is 50 nanoseconds, two more base delay
4 units should be added to frequency adjusted clock signal
5 `FREQ_CLK` during each concurrence period. Therefore, up/down
6 counter 2020 should contain the value 2. Thus, in general
7 up/down counter 2020 should be equal to the concurrence
8 period minus M times two times the base delay value.
9 However, during actual operation the information to
10 calculate the value for up/down counter 2020 is not
11 generally available. Therefore, searching techniques are
12 used to calculate the value for up/down counter 2020. A
13 searching technique in accordance with one embodiment of the
14 present invention is described below.

15 Up/down counter 2020 receives the value $M-1$ (i.e.,
16 multiplier M minus 1) on input terminals `IN[7:0]` via signals
17 `M_m1[7:0]`. Up/down counter 2020 provides both an output
18 value `OUT[7:0]` and a next value `NEXT[7:0]`. Output value
19 `OUT[7:0]` transitions on rising clock edges of control clock
20 `CTRL_CLK`. In contrast, next value `NEXT [7:0]` is equal to
21 the value that `OUT[7:0]` will become after the next rising
22 clock edge. Add delay signal `ADD_DELAY` is also provided to
23 control terminal `UP`. If add delay signal `ADD_DELAY` is
24 driven to the active logic level (i.e., logic high) up/down
25 counter 2020 counts up. Otherwise, up down/counter 2020
26 counts down.

27 To force modulo M counting, up/down counter 2020
28 includes a synchronous reset terminal coupled to the output
29 terminal of AND gate 2040. AND gate 2040, which receives
30 status signal `OUT=M_m1` and add delay control signal
31 `ADD_DELAY`, generates carry signal `CARRY`. Status signal
32 `OUT=M_m1` is driven to logic high when output value `OUT[7:0]`
33 is equal to multiplier M minus 1. Status signal `OUT=M_m1` is
34 typically generated by a comparator (not shown). Thus, if
35 up/down counter 2020 is counting up and output value
36 `OUT[7:0]` is equal to multiplier M minus 1, then up/down

1 counter 2020 is reset to zero on the next rising edge of
2 clock signal CTRL_CLK. Carry signal CARRY is also provided
3 to delay line register 1710. An active logic level (e.g.,
4 logic high) on carry signal CARRY enables delay line
5 register 1710 to increment.

6 Up/down counter 2020 also includes a load control
7 terminal LOAD coupled to the output terminal of AND gate
8 2050. AND gate 2050, which receives status signal OUT=ZERO
9 and add delay control signal ADD_DELAY through inverter
10 2060, generates borrow signal BORROW. Status signal
11 OUT=ZERO is driven to logic high when output value OUT[7:0]
12 is equal to zero. Status signal OUT=ZERO is typically
13 generated by a comparator (not shown). Thus, if up/down
14 counter 2020 is counting down and output value OUT[7:0] is
15 equal to zero, then up/down counter 2020 is configured to
16 load M minus 1. Borrow signal BORROW is also provided to
17 delay line register 1710. An active logic level (e.g.,
18 logic high) on Borrow signal BORROW enables delay line
19 register 1710 to decrement.

20 Next signal NEXT[7:0] is coupled to pulse input
21 terminals P_IN[7:0] of modulo-M delta-sigma circuit 2030.
22 Modulo-M delta sigma circuit 2030 also receives value M-1
23 (i.e., multiplier M minus 1) on modulo input terminals
24 M_IN[7:0] via signals M_m1[7:0], a pre-concurrence signal
25 PRE_CONC, and control clock signal CTRL_CLK. Modulo-M
26 delta-sigma circuit 2030, drives fine tuning increment
27 control signal FT_INC. For clarity, modulo-M delta sigma
28 circuit 2030 is said to receive a modulo value M (although
29 in the embodiment of Fig. 20, M minus 1 is actually
30 received) and a pulse count P. Pre-concurrence signal
31 PRE_CONC, which is provided to reset terminal RESET of
32 modulo-M delta sigma circuit 2030, is driven to the active
33 logic level (e.g., logic high) the clock cycle prior to a
34 concurrence. During M periods fine tuning increment
35 control signal FT_INC should contain P active pulses. The
36 active pulses on fine tuning increment control signal FT_INC

should be spread out across the M Periods. Table 3 provides some samples of fine tuning increment control signal FT_INC, where a "1" represents an active pulse and "0" represents an inactive pulse.

TABLE 3

M	P	FT_INC
4	2	1010
6	2	100100
6	3	101010
6	5	111110
7	3	1010100
7	4	1101010
9	4	101010100
12	5	101010010100
15	3	100001000010000

Concurrence

Fig. 21 is a block diagram of modulo-M delta sigma circuit 2030 in accordance with one embodiment of the present invention. The embodiment of Fig. 21 includes an incrementer 2105, a multiplier 2110, a subtracter 2120, an adder 2130, a multiplexing circuit 2140, a latch 2150, and a comparator 2160. Modulo input terminals M_IN[7:0] are coupled to an input port IN of incrementer 2105, a second input port IN2 of multiplexing circuit 2140, and a second input port IN2 of comparator 2160. Because the specific embodiment of Fig. 21 is designed to receive modulo value M minus 1 rather than modulo value M on modulo input terminals M_IN[7:0], incrementer 2105 increments the value provided on modulo input terminals M_IN[7:0] by one to generate modulo value M, which is provided to a first input port of multiplier 2110. Other embodiments of the present invention may receive modulo value M on modulo input terminals M_IN[7:0]. These embodiments would not require incrementer 2105. A second input port IN2 of multiplier 2110 is coupled to an output terminal of comparator 2160. Multiplier 2110

1 multiplies the value provided on modulo input terminals
2 M_IN[7:0] by the output value of comparator 2160 to generate
3 an output product, which is provided to a second input port
4 IN2 of subtracter 2120. In many embodiments of the present
5 invention, multiplier 2110 is implemented using a plurality
6 of AND gates, because the output value of comparator 2160 is
7 a single bit.

8 Pulse input terminals P_IN[7:0] are coupled to a first
9 input terminal of subtracter 2120. Subtracter 2120 is
10 configured to subtract the output value from multiplier 2110
11 from the pulse value provided on pulse input terminals
12 P_IN[7:0] to generate a delta value DELTA on output port OUT
13 of subtracter 2120. Output port OUT of subtracter 2120 is
14 coupled to a first input port IN1 of adder 2130. A second
15 input port IN2 of adder 2130 is coupled to an output port
16 OUT of latch 2150. Adder 2130 is configured to add delta
17 value DELTA provided by subtracter 2120 to a latch value
18 LATCH provided by latch 2150 to generate a sigma value SIGMA
19 on output port OUT of adder 2130. Output port OUT of adder
20 2130 is coupled to a first input port IN1 of multiplexing
21 circuit 2140. Some embodiments of the present invention
22 calculate sigma value SIGMA using a sigma calculation
23 circuit, such as a three input adder, which can perform the
24 calculation faster than using a separate delta calculation
25 circuit, such as subtracter 2120. In these embodiments the
26 sigma calculation circuit replaces subtracter 2120 and adder
27 2130. For embodiments using a three input adder, the output
28 value of multiplier 2110 can be converted into a 2's
29 complement format prior to the three input adder.
30 Furthermore, incrementer 2105 and multiplier 2110 may be
31 combined within a circuit to compute the 2's complement
32 format.

33 Multiplexing circuit 2140 is configured to drive either
34 sigma value SIGMA or the value provided on modulo input
35 terminals M_IN[7:0] to input port IN of latch 2150 through
36 output port OUT of multiplexing circuit 2140. Reset

terminal RESET is coupled to a control terminal of multiplexing circuit 2140. Pre-concurrence signal PRE_CONC, which is coupled to reset terminal RESET in Fig. 20, determines the output value of multiplexing circuit 2140. Specifically, during the clock cycle before concurrences multiplexing circuit 2140 is configured to drive the value provided on modulo input terminals M_IN[7:0] to input port IN of latch 2150. Otherwise, multiplexing circuit 2140 is configured to drive sigma value SIGMA to input port IN of latch 2150. Latch 2150, which is clocked by control clock signal CTRL_CLK, provides a LATCH value on output port OUT of latch 2150 to a first input port IN1 of comparator 2160. Comparator 2160, which is configured to compare latch value LATCH with the value provided on modulo input terminals M_IN[7:0], generates fine tuning increment signal FT_INC on output terminal OUT of comparator 2160. Specifically, if latch value LATCH is greater than the modulo value provided on modulo input terminals M_IN[7:0], fine tuning increment signal FT_INC is driven to the active logic level (e.g., logic high). Otherwise, fine tuning increment signal FT_INC is driven to the inactive logic level (e.g., logic low).

Table 4 provides a pseudo code implementation of a second embodiment of modulo-M delta sigma circuit 2030. One skilled in the art of digital design can convert the pseudo code of Table 4 to a hardware definition language such as Verilog to implement the circuit.

TABLE 4

```

DELTA = P - (FT_INC * M)
SIGMA = DELTA + LATCH
IF RESET then LATCH=(M-1)
    else LATCH=SIGMA
IF LATCH > (M-1) then FT_INC = 1
    else FT_INC = 0

```

As explained above, one embodiment of the present invention operates digital frequency synthesizer 1400 in

1 three distinct phases. Specifically, digital frequency
2 synthesizer 1400 is operated in a coarse frequency search
3 phase, a fine frequency search phase, and a clock
4 maintenance phase. During the coarse frequency search
5 phase, variable delay line 1520 (Fig. 15) is configured
6 using the fast binary search as described above. Delay line
7 fine tuning controller 1720 (Fig. 17) is disabled during the
8 coarse frequency search phase. The coarse frequency search
9 phase ends when right shifter 1830 (Fig. 18) contains a
10 value of one.

11 During the fine frequency search phase, delay line fine
12 tuning controller 1720 is activated and clock selector 1430
13 (Fig. 14) is configured to select frequency adjusted clock
14 signal FREQ_CLK as the control clock signal CTRL_CLK.
15 During the fine frequency search phase, delay line fine
16 tuning controller 1720 is controlled by frequency comparator
17 1850 (Fig. 18) using control signal A/!S as described above.
18 Specifically, control signal A/!S determines whether up/down
19 counter 2020 increments or decrements. Halt/restart circuit
20 1445 is also used in the fine frequency search phase during
21 each concurrence period. In the fine frequency search
22 phase, up/down counter 2020 increments or decrements by one
23 each concurrence period. As explained above, up/down
24 counter 2020 is linked to delay line register 1710 by carry
25 signal CARRY and borrow signal BORROW. Thus, the value in
26 delay line register 1710 may change during the fine
27 frequency search phase. The fine frequency search phase
28 ends when frequency comparator 1850 detects a reversal and
29 drives frequency comparator reversal signal to the active
30 state.

31 During the clock maintenance phase, phase comparator
32 1440 (Fig. 14) takes control of oscillator control circuit
33 1460 from initialization circuit 1450. During the
34 maintenance phase, delay line fine tuning controller 1720 is
35 selectively enabled. Specifically, in one embodiment of the
36 present invention, the maintenance phase cycles through

three sub-phases. Each sub-phase lasts for one concurrence period. In the first sub-phase, phase comparator 1440 is initialized. During the first sub-phase the value of up/down counter 2020 does not change. In the second sub-phase phase comparator 1440 determines whether feedback clock signal FBK_CLK leads or lags divided synchronizing clock signal D_SYNCH_CLK. In the third sub-phase delay line fine tuning controller 1720 is enabled. Thus, up/down counter 2020 can increment or decrement by one as controlled by phase comparator control signal PC_CTRL. As explained above phase comparator control signal PC_CTRL indicates whether feedback clock signal FBK_CLK leads or lags divided synchronizing clock signal D_SYNCH_CLK. If delayed synchronizing clock signal D_SYNCH_CLK leads feedback clock signal FBK_CLK, then phase comparator 1440 causes up/down counter 2020 to decrement during the second sub-phase. Otherwise, phase comparator 1440 causes up/down counter 2020 to increment during the second sub-phase. In other embodiments, the maintenance phase may include more or fewer sub-phases. For example, in one embodiment, the first sub-phase and the second sub-phase described above are combined into a single sub-phase. Some embodiments of the present invention wait until phase comparator 1440 detects multiple reversals (such as four reversals) before declaring frequency adjusted clock signal FREQ_CLK is at selected frequency F_SEL.

In the various embodiments of the present invention, novel structures have been described for digital clock managers. By using a synchronizing clock signal with matched output delays, the present invention can provide deskewed output clock signals with synchronized frequency adjusted clock signals. The various embodiments of the structures and methods of this invention that are described above are illustrative only of the principles of this invention and are not intended to limit the scope of the invention to the particular embodiments described. For

1 example, in view of this disclosure those skilled in the art
2 can define other delay lock loops, output generation
3 circuits, output delays, variable delay circuits, digital
4 frequency synthesizers, clock phase shifters, delay lines,
5 output generators, controllers, phase detectors, latches,
6 registers, clock dividers, phase comparators, frequency
7 comparators, up/down counters, initialization circuits,
8 delta-sigma circuits, latches, halt/restart circuits, delay
9 lines, variable digital oscillators, edge-triggered SR
10 circuits, active edges, enable logic levels, and so forth,
11 and use these alternative features to create a method,
12 circuit, or system according to the principles of this
13 invention. Thus, the invention is limited only by the
14 following claims.

1 CLAIMS

2
3 What is claimed is:

4 1. A digital clock manager having a reference input
5 terminal, a skew input terminal, an output terminal, and a
6 frequency adjusted output terminal, the digital clock
7 manager comprising:

8 a delay lock loop (DLL) coupled to the reference
9 input terminal, the skew input terminal, and the output
10 terminal; and

11 a digital frequency synthesizer, coupled to the
12 delay lock loop and the frequency adjusted output
13 terminal.

14
15 2. The digital clock manager of Claim 1, wherein the
16 delay lock loop is configured to generate an output clock
17 signal on the output terminal which synchronizes a reference
18 clock signal on the reference input terminal with a skewed
19 clock signal on the skew input terminal.

20
21 3. The digital clock manager of Claim 1, wherein the
22 digital frequency synthesizer is configured to generate a
23 frequency adjusted clock signal on the frequency adjusted
24 output terminal and wherein the frequency adjusted clock
25 signal is synchronized with the output clock signal during
26 concurrences.

27
28 4. The digital clock manager of Claim 1, wherein the
29 delay lock loop comprises a DLL output circuit having a DLL
30 output delay.

31
32 5. The digital clock manager of Claim 4, wherein the
33 digital frequency synthesizer comprises a DFS output circuit
34 having a DFS output delay.

1 6. The digital clock manager of Claim 5, wherein the
2 DLL output delay is substantially equal to the DFS output
3 delay.

4
5 7. The digital clock manager of Claim 5, wherein the
6 DLL output circuit comprises a plurality of components and
7 the DFS output circuit comprises the same plurality of
8 components.

9
10 8. The digital clock manager of Claim 1, wherein the
11 delay lock loop drives a synchronizing clock signal to the
12 digital frequency synthesizer.

13
14 9. The digital clock manager of Claim 8, wherein the
15 delay lock loop is configured to generate an output clock
16 signal on the output terminal, wherein the output clock
17 signal lags the synchronizing clock signal by a DLL output
18 delay.

19
20 10. The digital clock manager of Claim 9, wherein the
21 digital frequency synthesizer is configured to generate a
22 frequency adjusted clock signal on the frequency adjusted
23 output terminal, wherein an active edge of the frequency
24 adjusted clock signal lags an active edge of the
25 synchronizing clock signal by a DFS output delay during a
26 concurrence period.

27
28 11. The digital clock manager of Claim 10, wherein the
29 DLL output delay is substantially equal to the DFS output
30 delay.

31
32 12. The digital clock manager of Claim 1, further
33 comprising a variable delay circuit coupled between the
34 delay lock loop and the output terminal.

1 13. The digital clock manager of Claim 1, further
2 comprising a variable delay circuit coupled between the
3 digital frequency synthesizer and the frequency adjusted
4 output terminal.

5
6 14. The digital clock manager of Claim 1, further
7 comprising a multiplexer having a first input terminal
8 coupled to the reference input terminal, a second input
9 terminal coupled to the delay lock loop, and an output
10 terminal coupled to the digital frequency synthesizer.

11
12 15. The digital clock manager of Claim 1, wherein the
13 delay lock loop is configured to provide a synchronizing
14 clock signal to the second input terminal of the
15 multiplexer.

16
17 16. The digital clock manager of Claim 15, wherein the
18 digital frequency synthesizer is configured to perform a
19 frequency search phase using a reference clock signal
20 provided to the reference input terminal.

21
22 17. The digital clock manager of Claim 16, wherein the
23 digital frequency synthesizer is configured to provide a
24 frequency adjusted clock signal based on the synchronizing
25 clock signal.

26
27 18. The digital clock manager of Claim 1, wherein the
28 digital frequency synthesizer performs a frequency search
29 while the delay lock loop is performing lock acquisition.

30
31 19. A method to generate an output clock signal and a
32 frequency adjusted clock signal from a reference signal,
33 wherein the output clock signal is synchronized with the
34 frequency adjusted clock signal during a concurrence; the
35 method comprising:

36 generating a synchronizing clock signal;

1 matching a DLL output delay with a DFS output
2 delay;
3 generating the output clock signal lagging the
4 synchronizing clock signal by the DLL output delay; and
5 generating the frequency adjusted clock signal so
6 that an active edge of the frequency adjusted clock
7 signal lags an active edge of the synchronizing clock
8 signal by the DFS output delay during the concurrence.
9

10 20. The method of Claim 19, wherein the step of
11 matching a DLL output delay with a DFS output delay
12 comprises synchronizing a DLL output circuit with a DFS
13 output circuit.
14

15 21. The method of Claim 19, further comprising
16 performing lock acquisition.
17

18 22. The method of Claim 21, further comprising
19 performing a frequency search during lock acquisition.

1 SYNCHRONIZED MULTI-OUTPUT DIGITAL CLOCK MANAGER

2
3 John D. Logue

4 Andrew K. Percey

5 F. Erich Goetting
6
78 ABSTRACT OF THE DISCLOSURE

9 A digital clock manager is provided. The digital clock
10 manager generates an output clock signal that causes a
11 skewed clock signal to be synchronized with a reference
12 clock signal. Furthermore, the digital clock manager
13 generates a frequency adjusted clock signal that is
14 synchronized with the output clock signal during concurrence
15 periods. The digital clock manager includes a delay lock
16 loop and a digital frequency synthesizer. The delay lock
17 loop generates a synchronizing clock signal that is provided
18 to the digital frequency synthesizer. The output clock
19 signal lags the synchronizing clock signal by a DLL output
20 delay. Similarly, the frequency adjusted clock signal lags
21 the synchronizing clock signal by a DFS output delay. By
22 matching the DLL output delay to the DFS output delay, the
23 digital clock manager synchronizes the output clock signal
24 and the frequency adjusted clock signal.

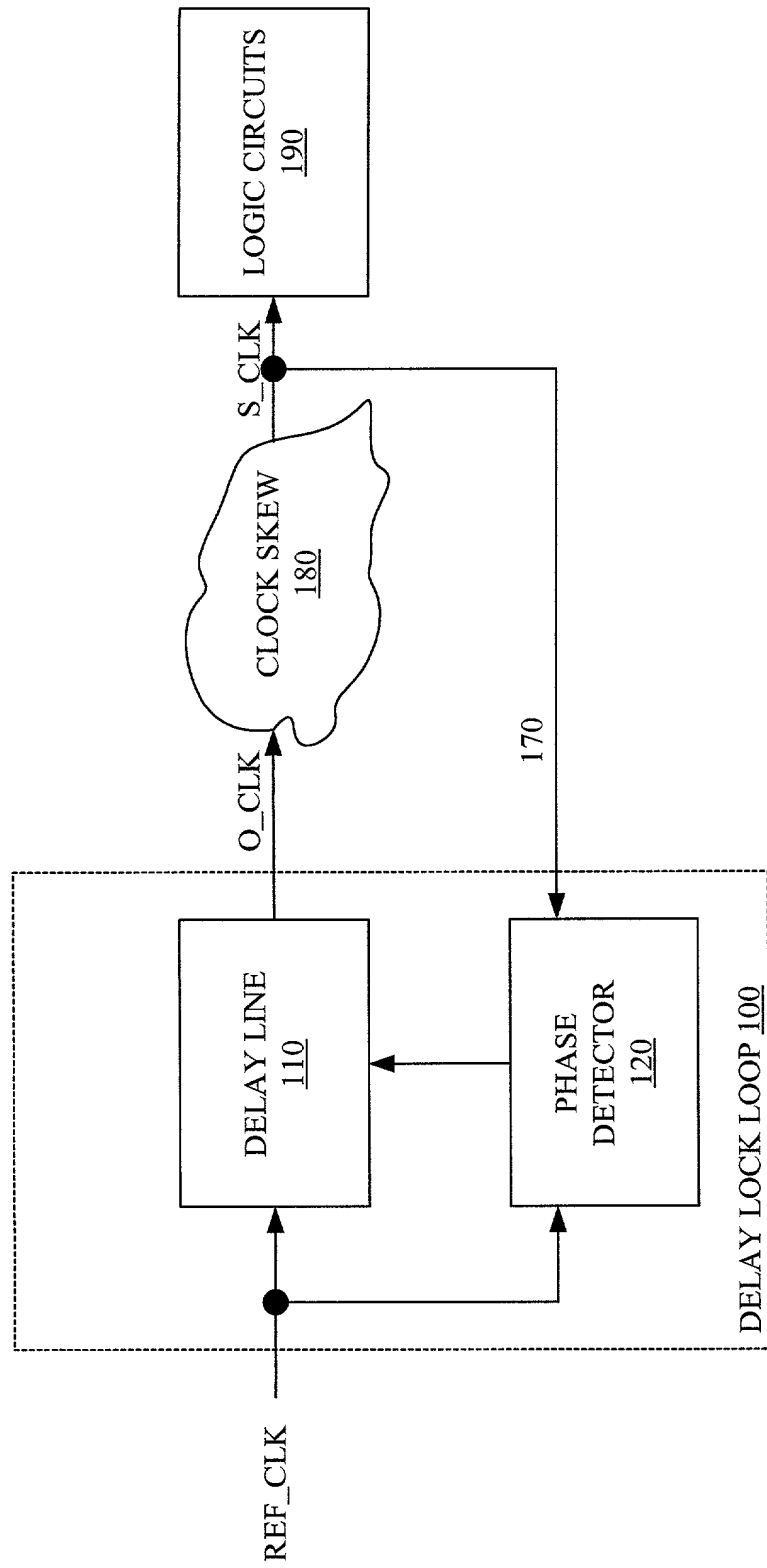


FIGURE 1 (Prior Art)

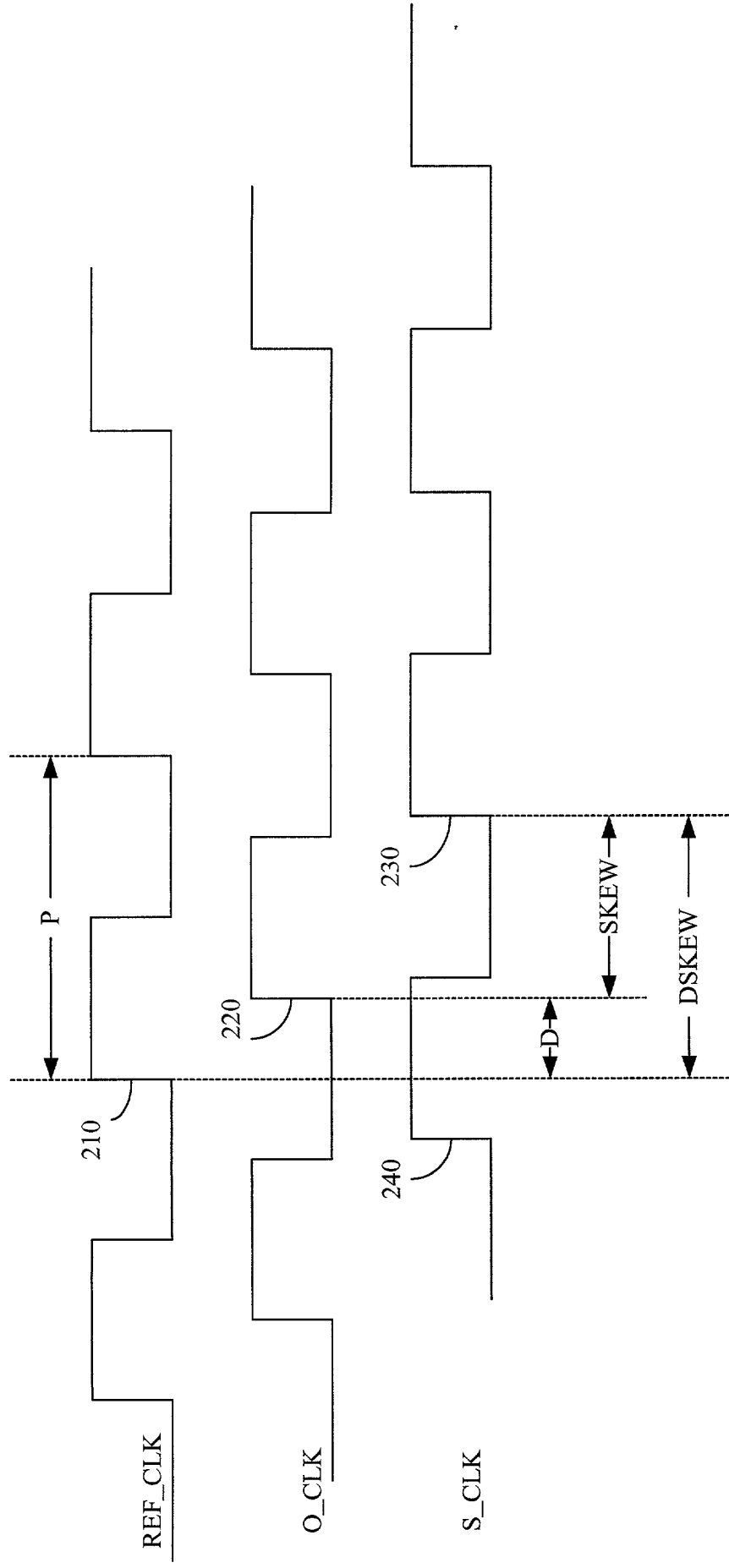


FIGURE 2(a)

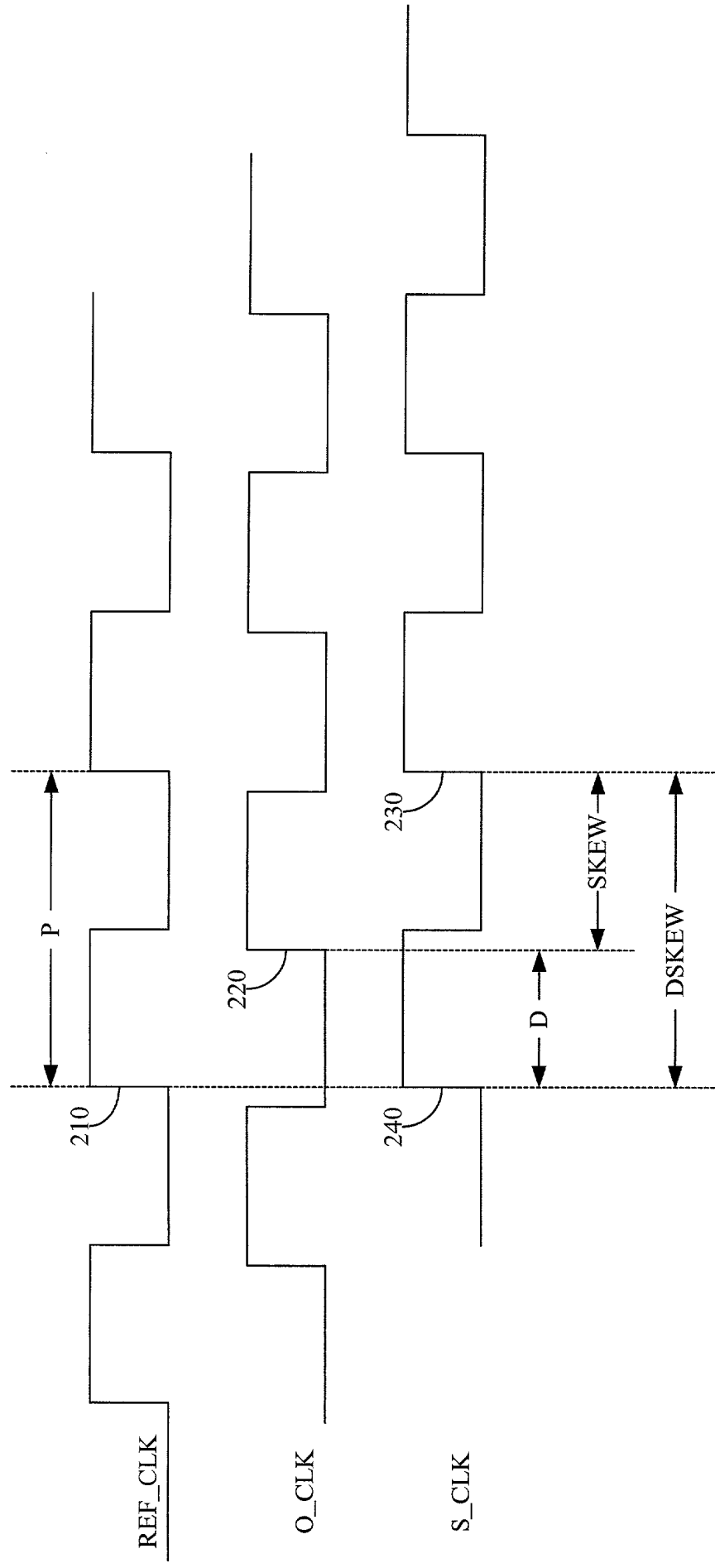


FIGURE 2(b)

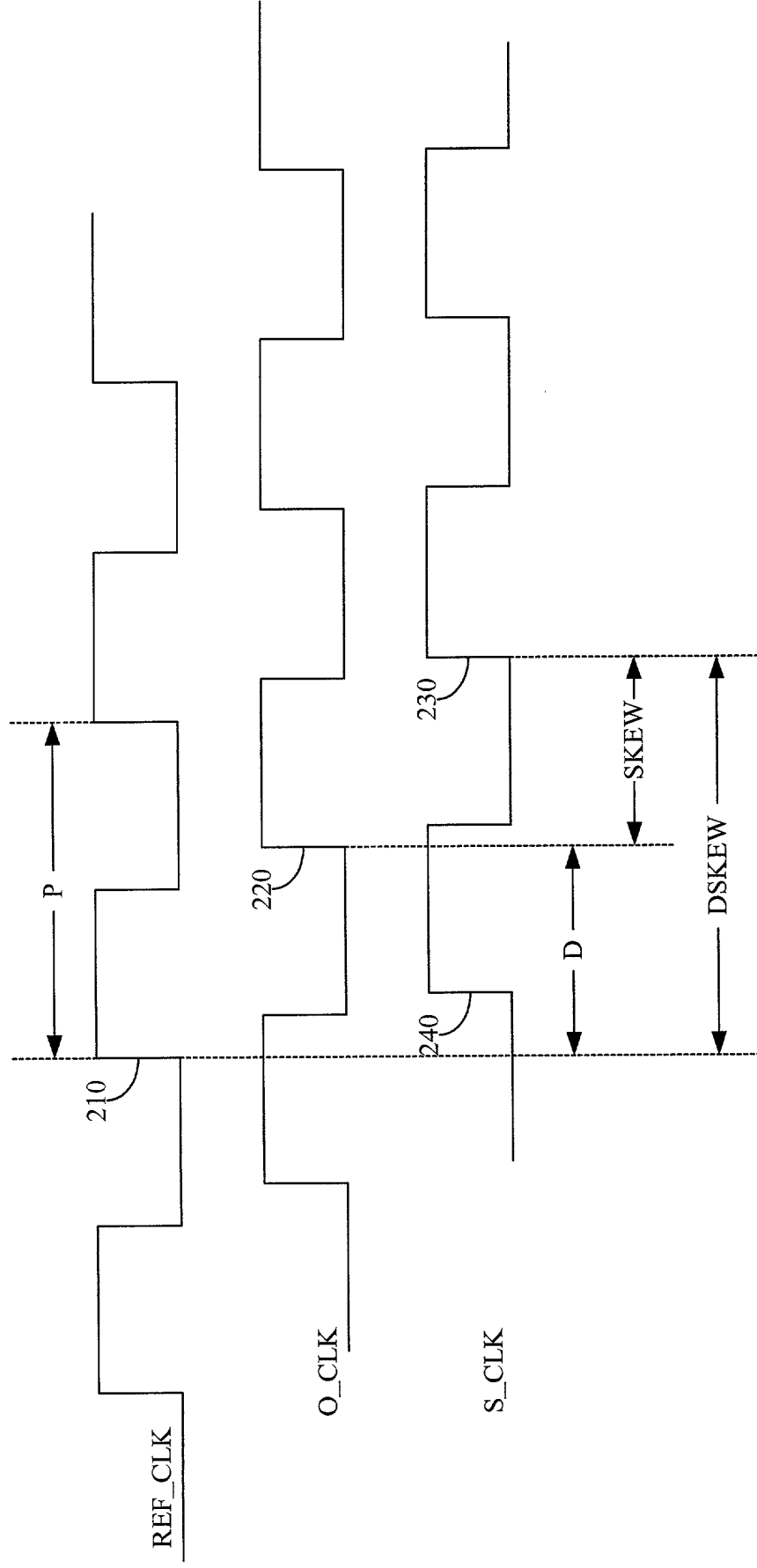


FIGURE 2(c)

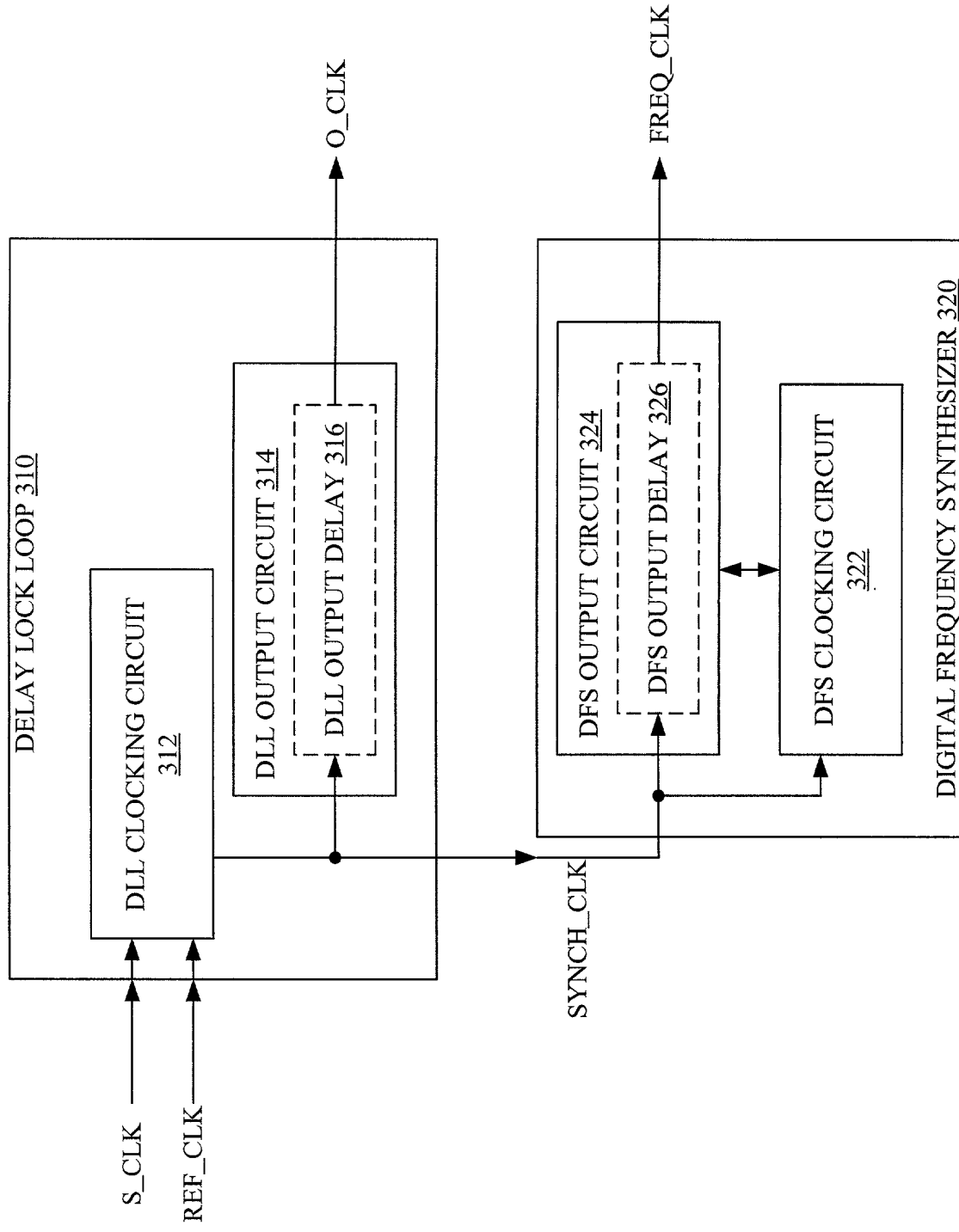


FIGURE 3

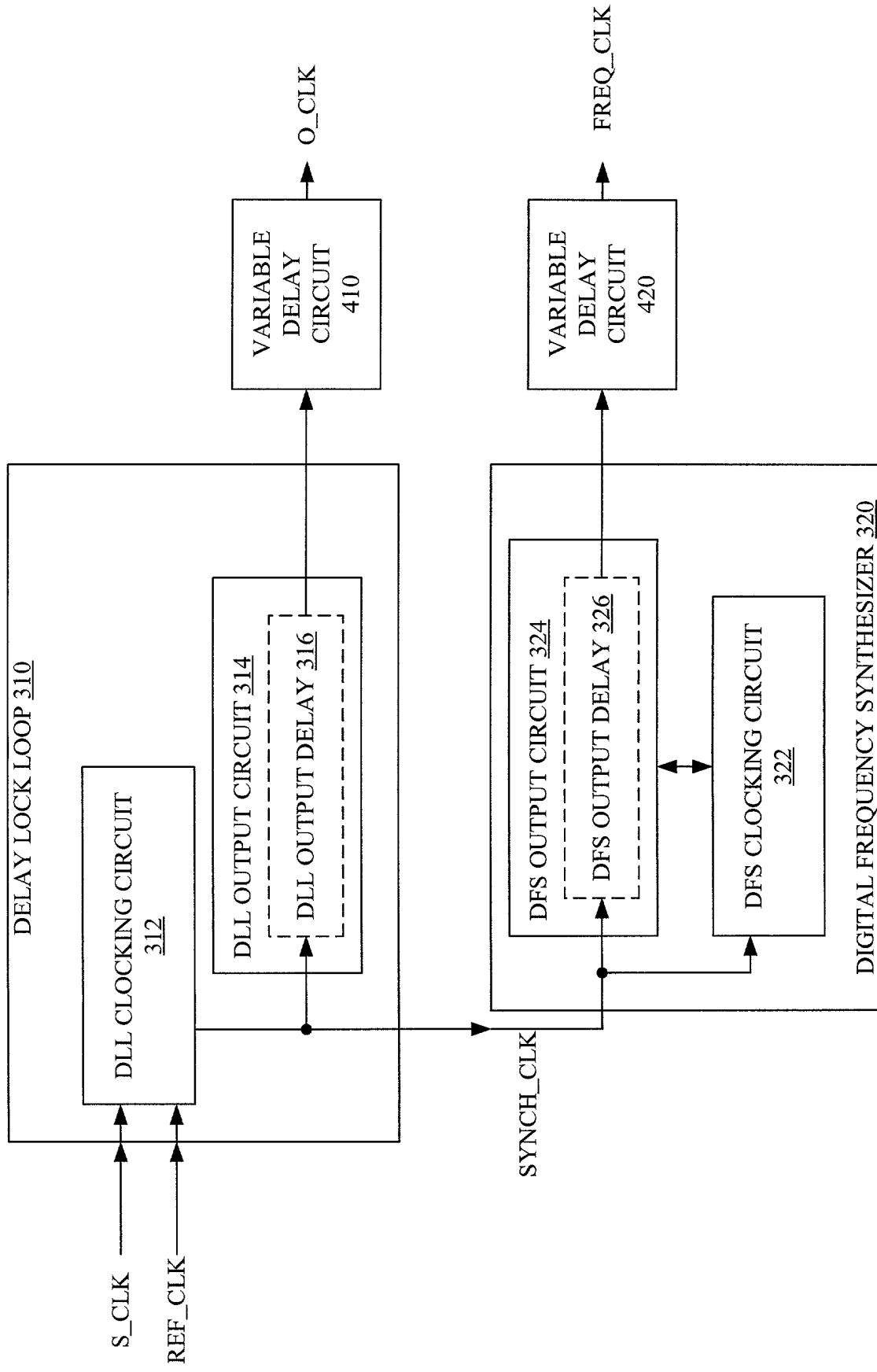


FIGURE 4

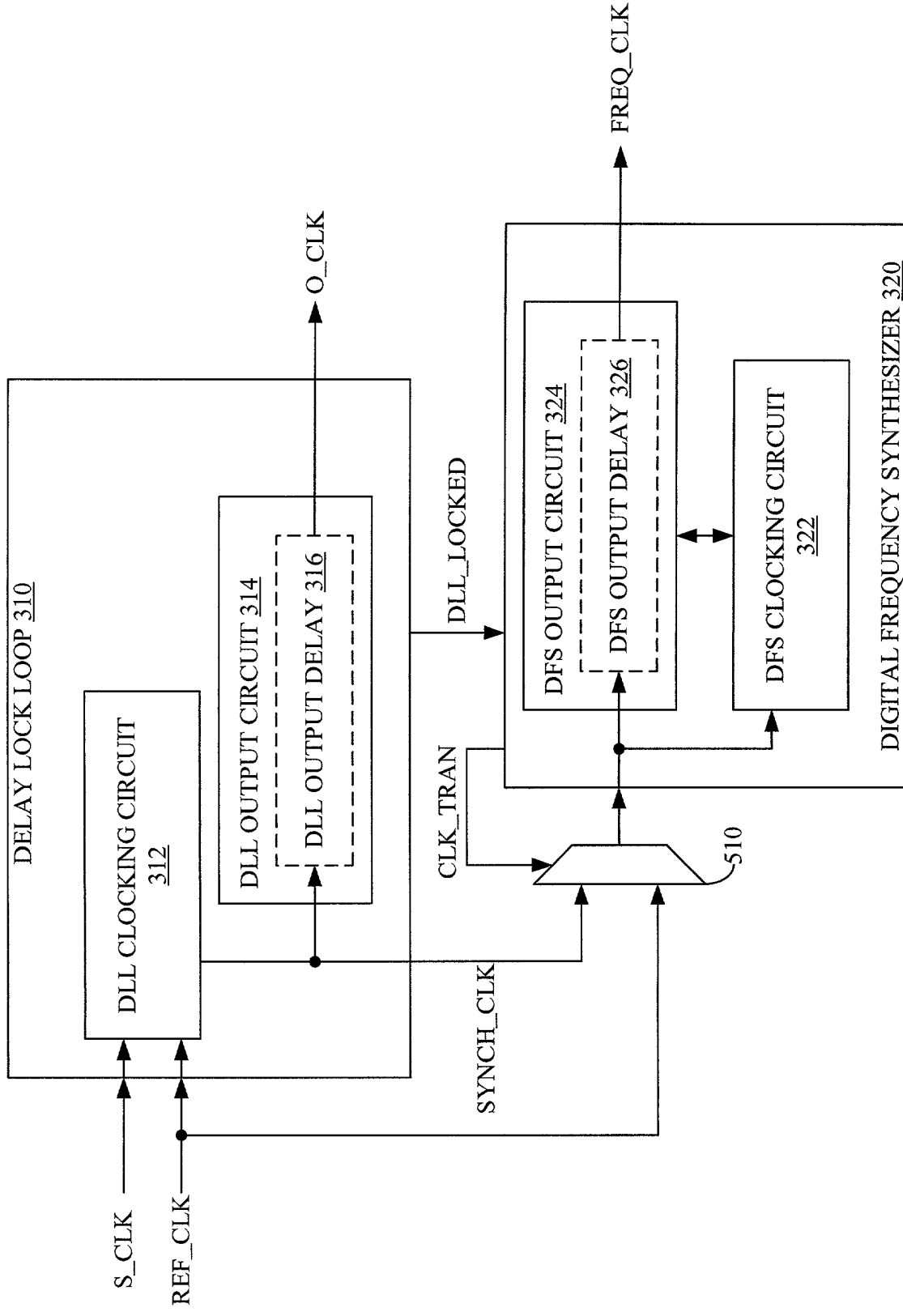


FIGURE 5

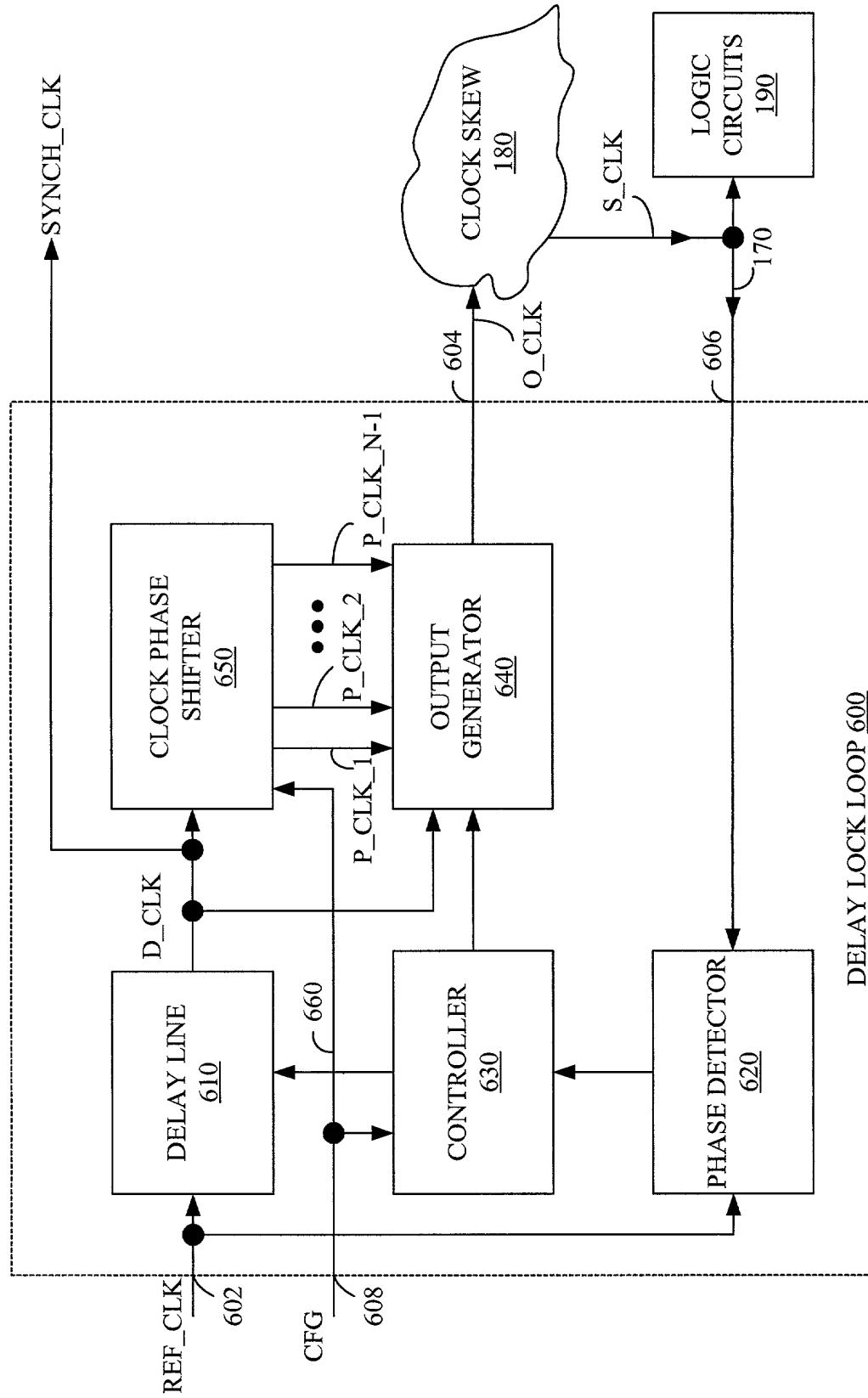


FIGURE 6

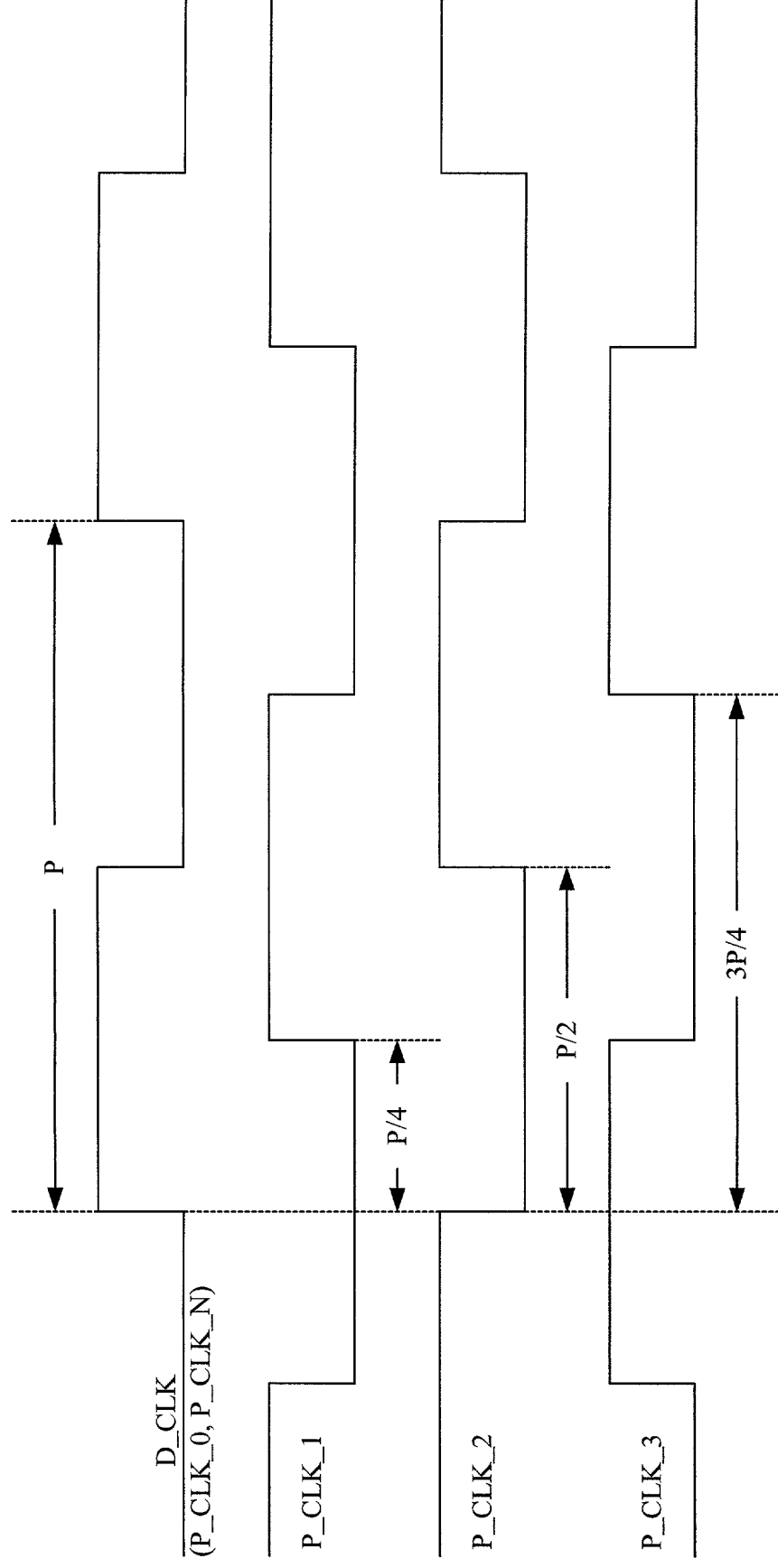


FIGURE 7

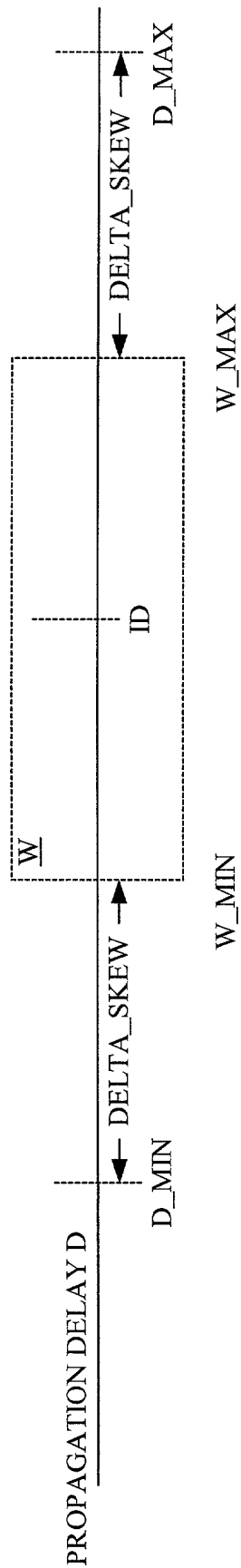


FIGURE 8

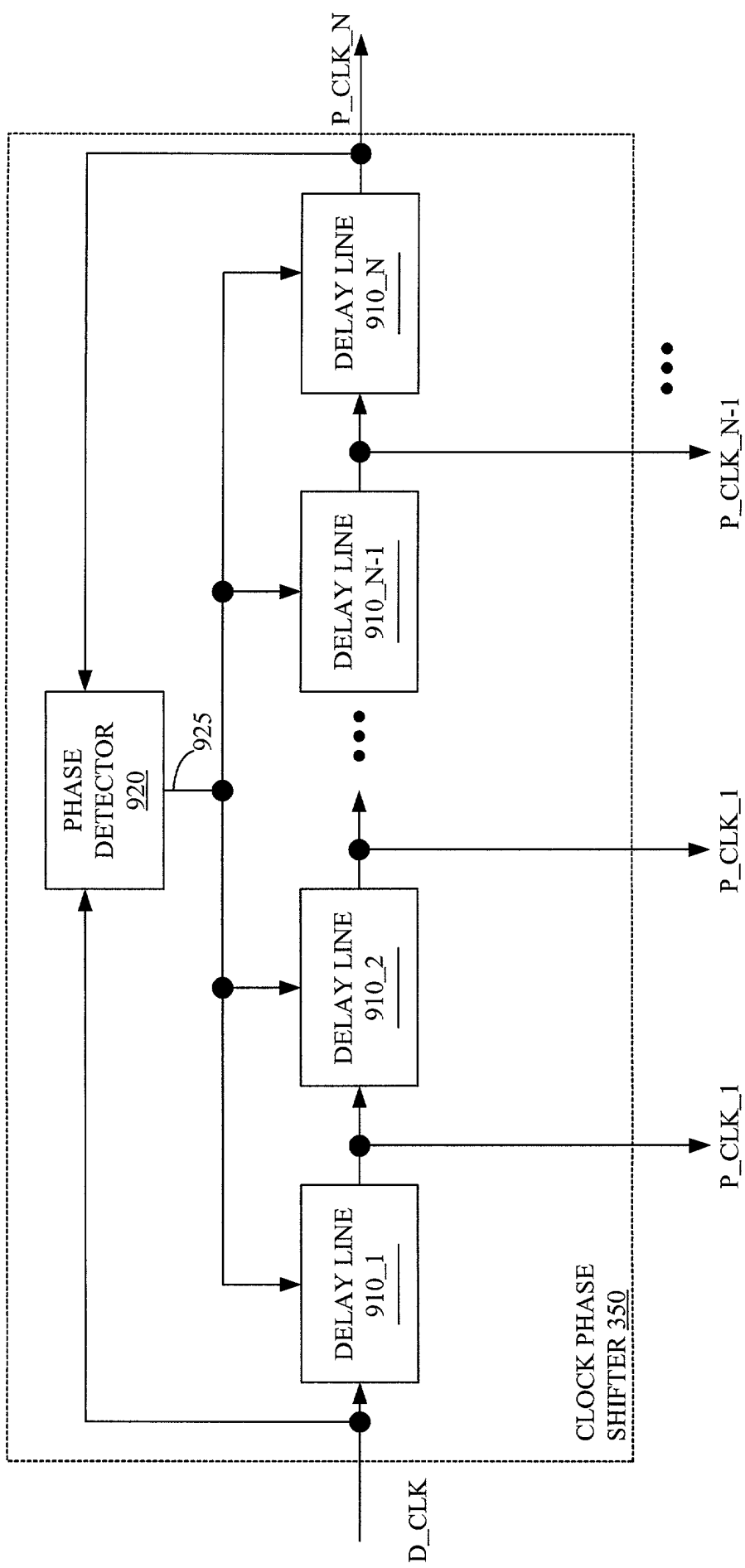


FIGURE 9

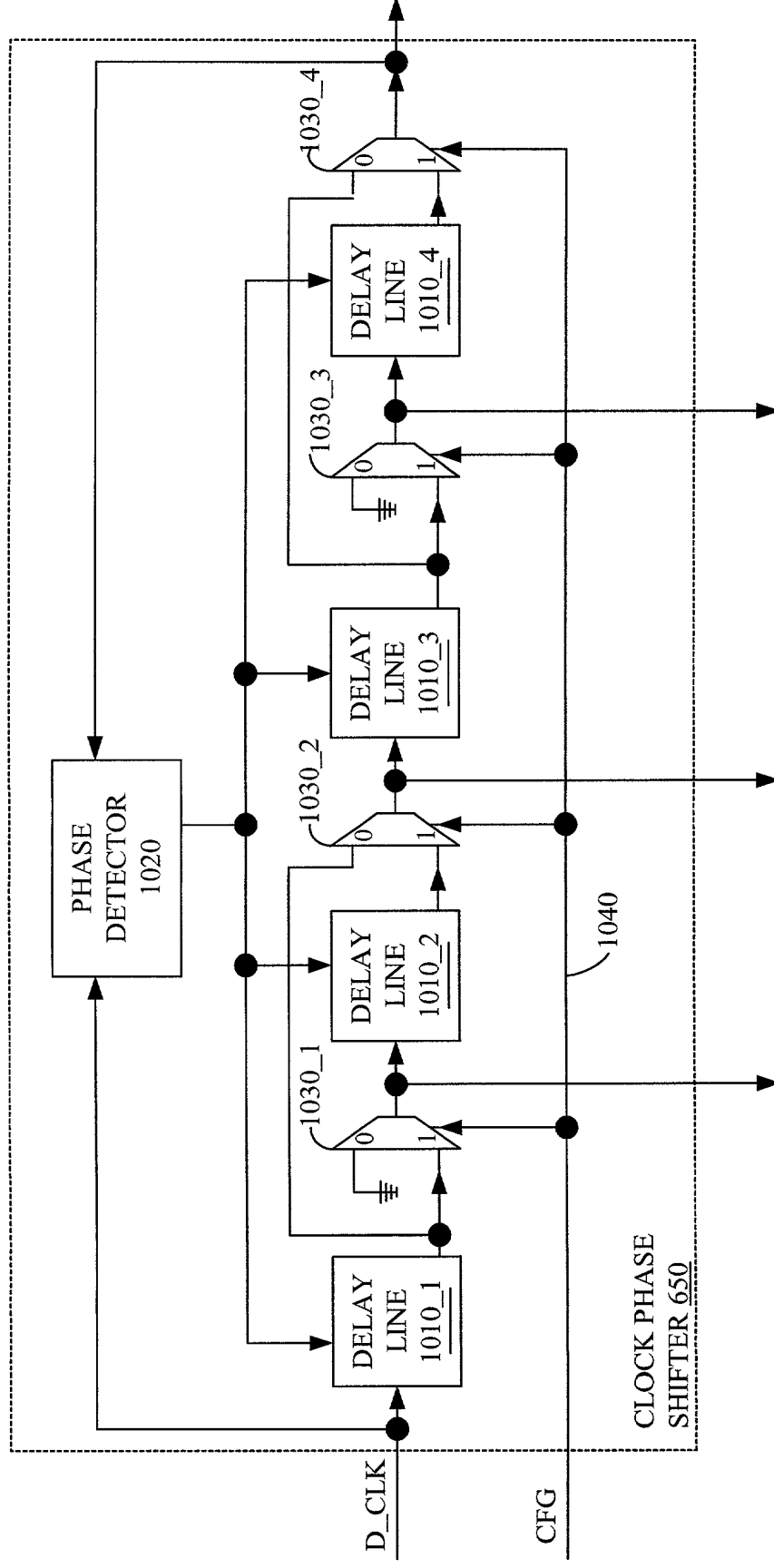


FIGURE 10

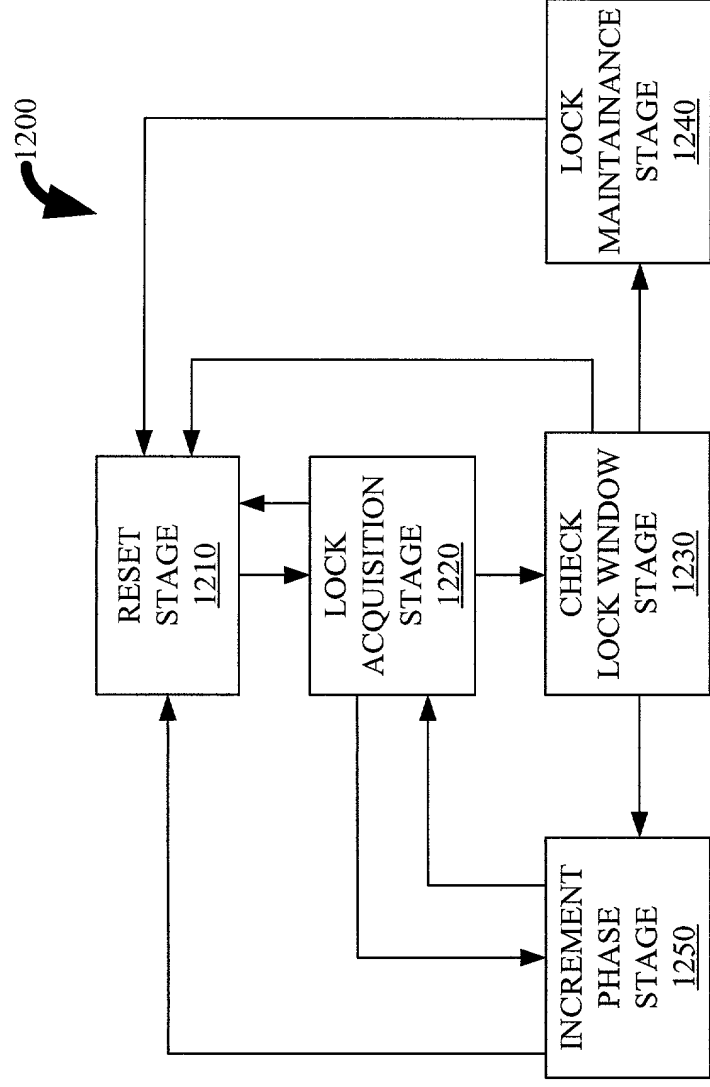


FIGURE 12

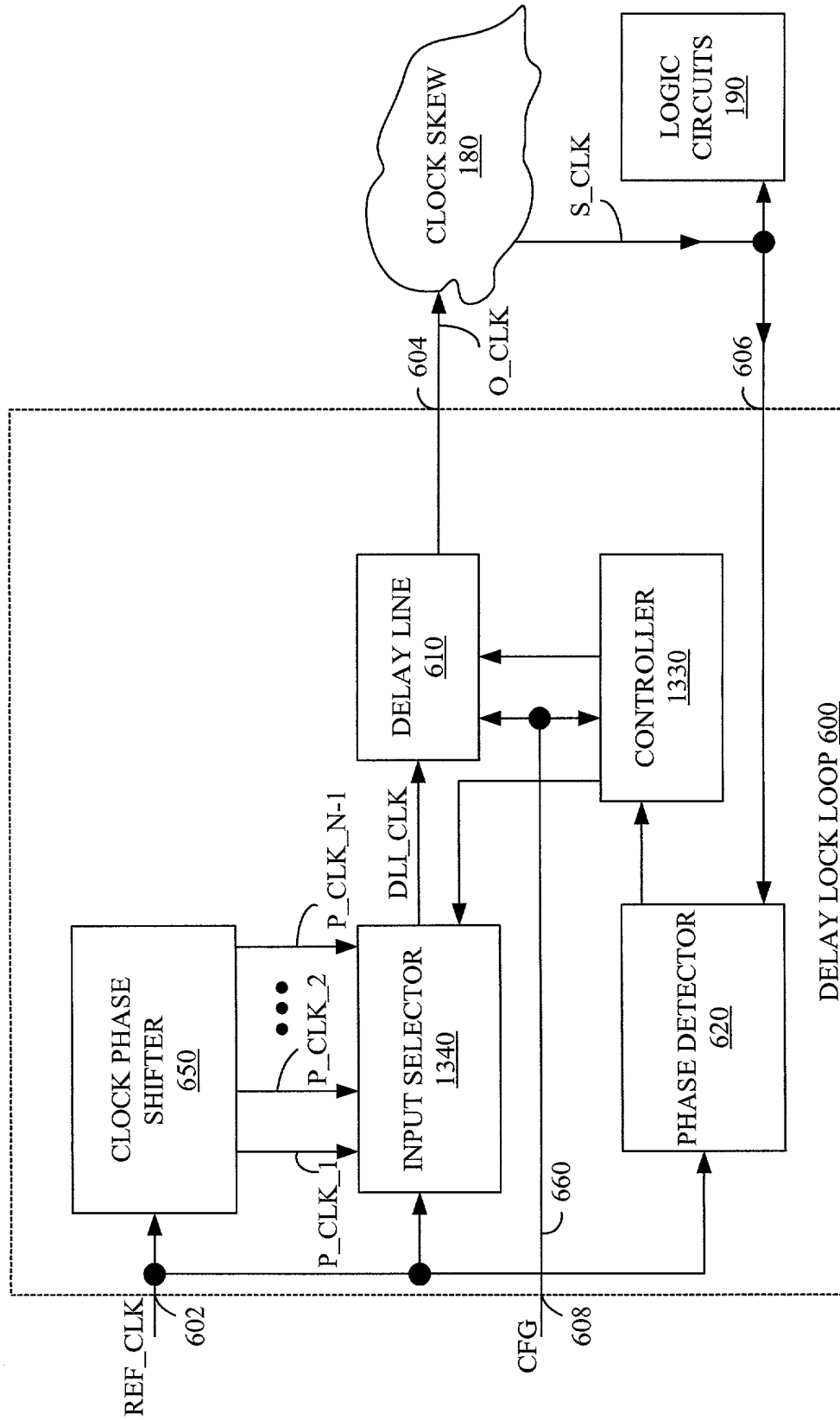


FIGURE 13

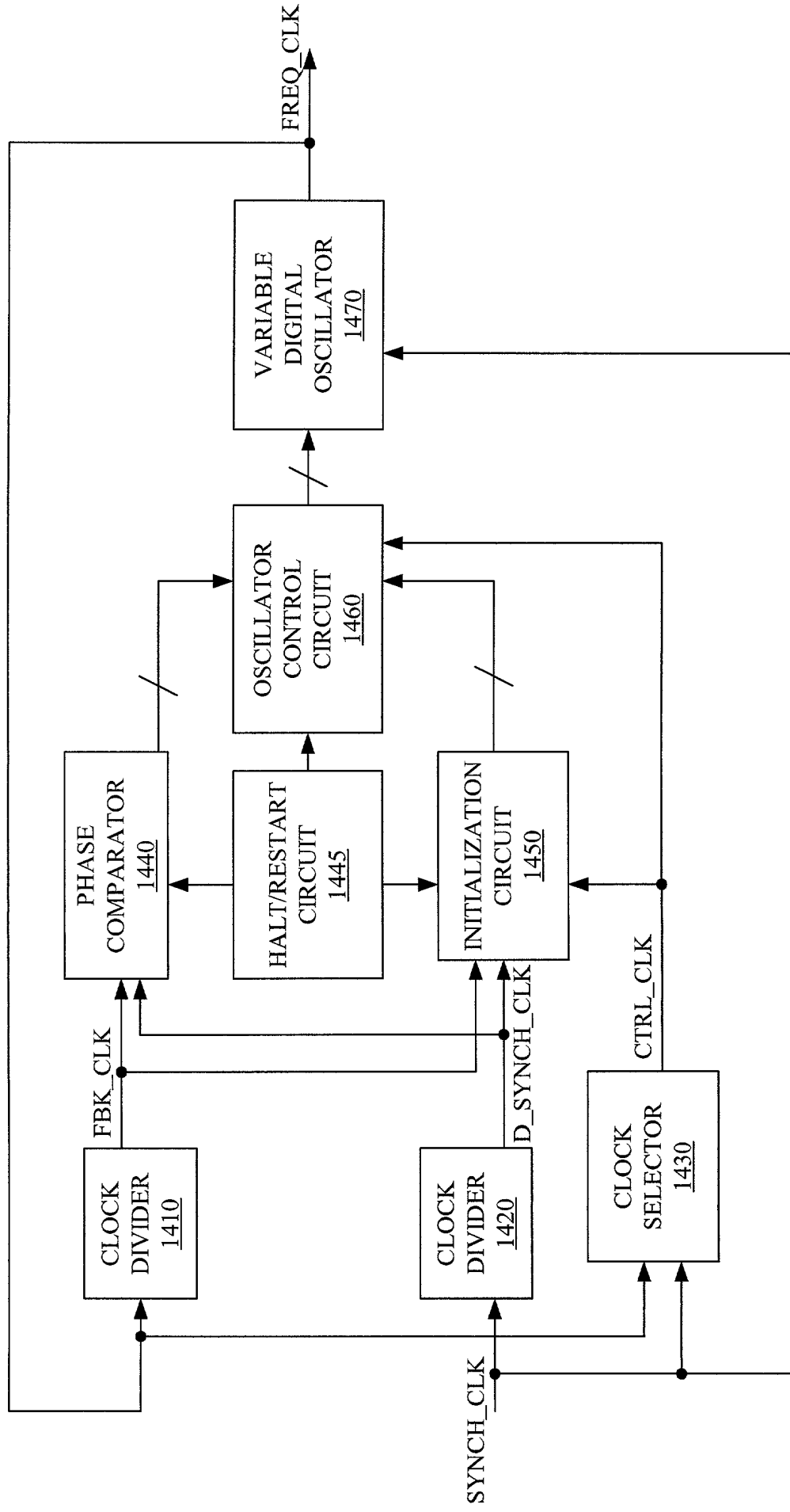


FIGURE 14(a)

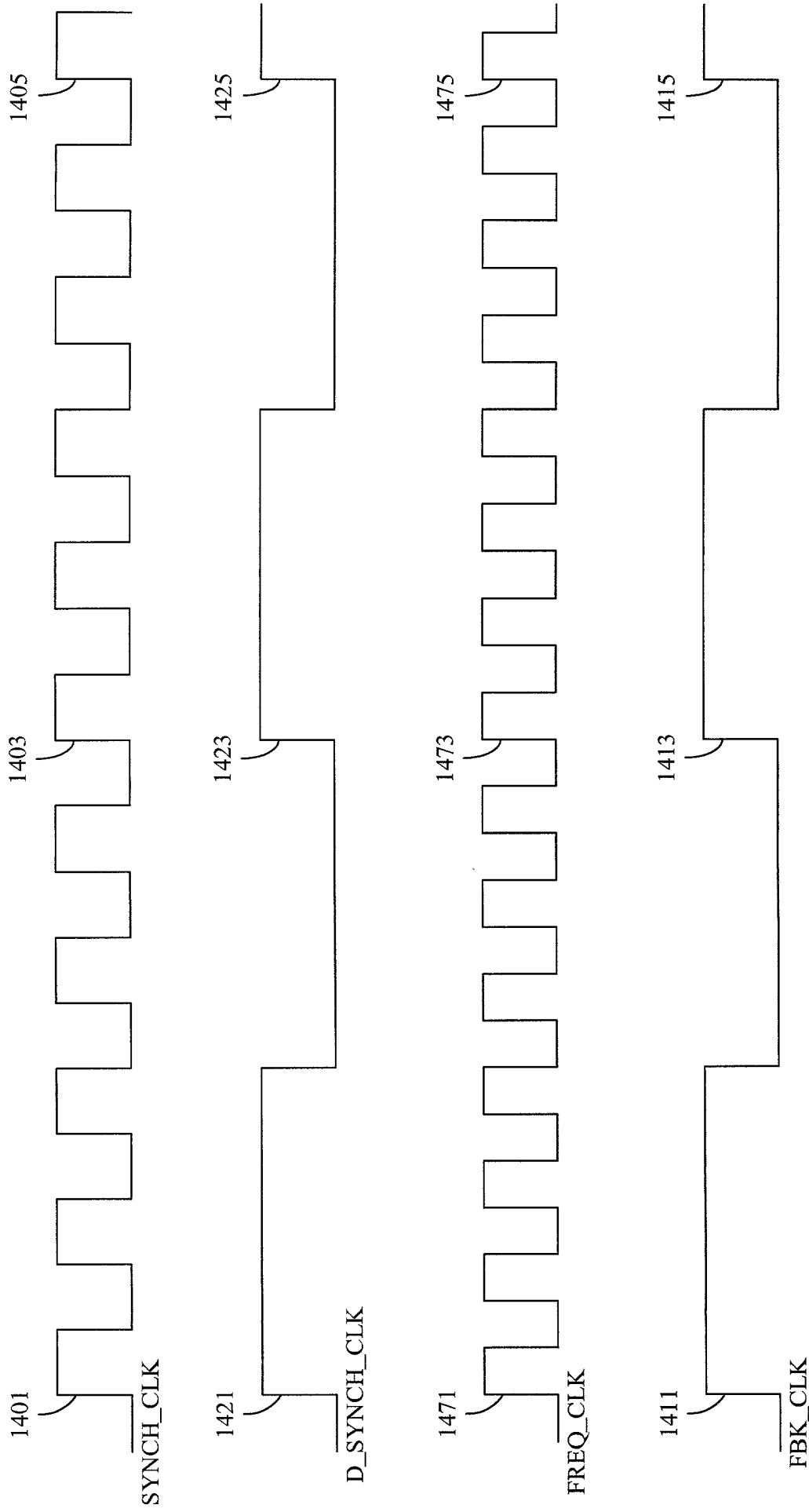


FIGURE 14(b)

output" 6248960
1470

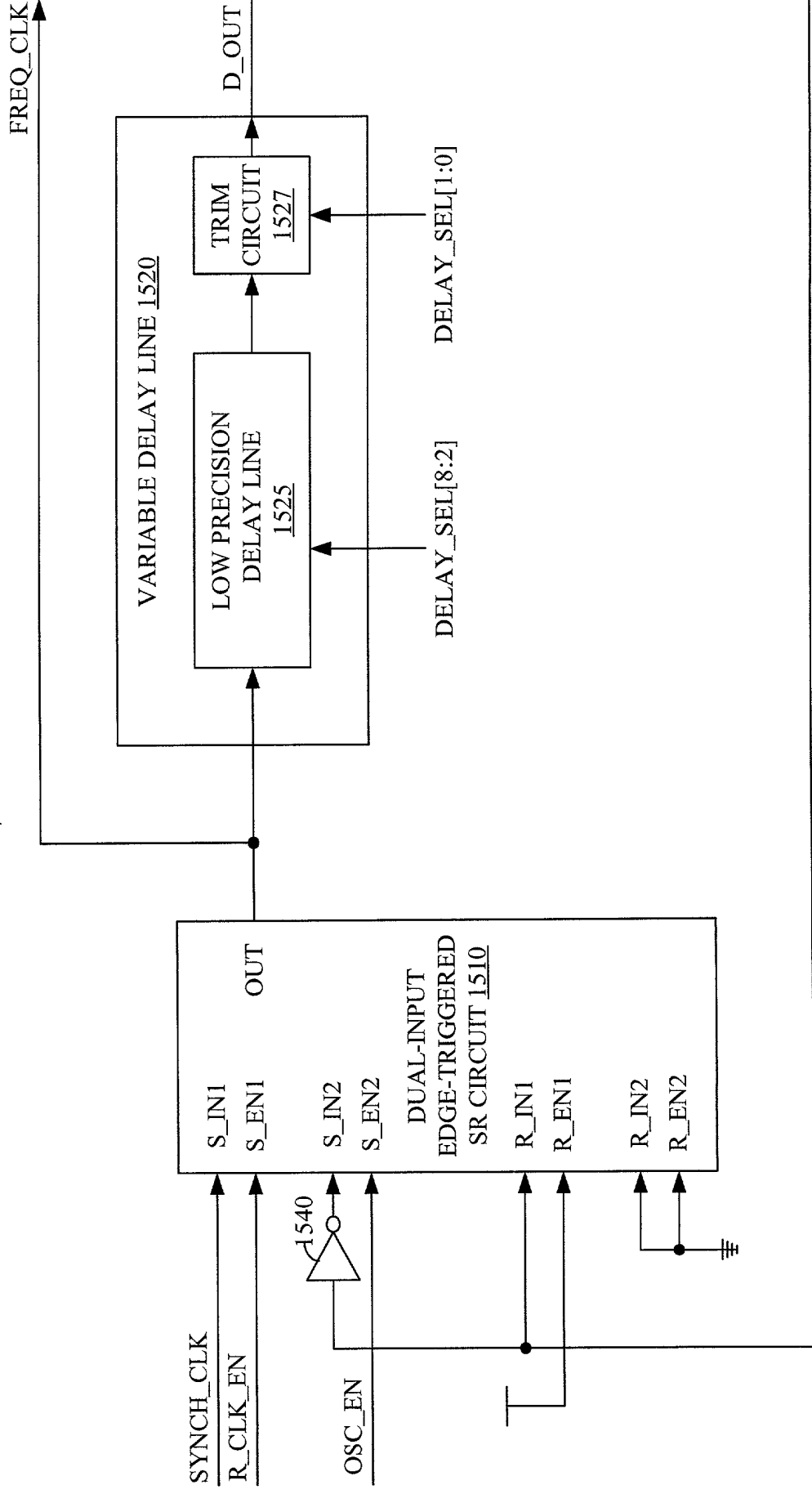


FIGURE 15

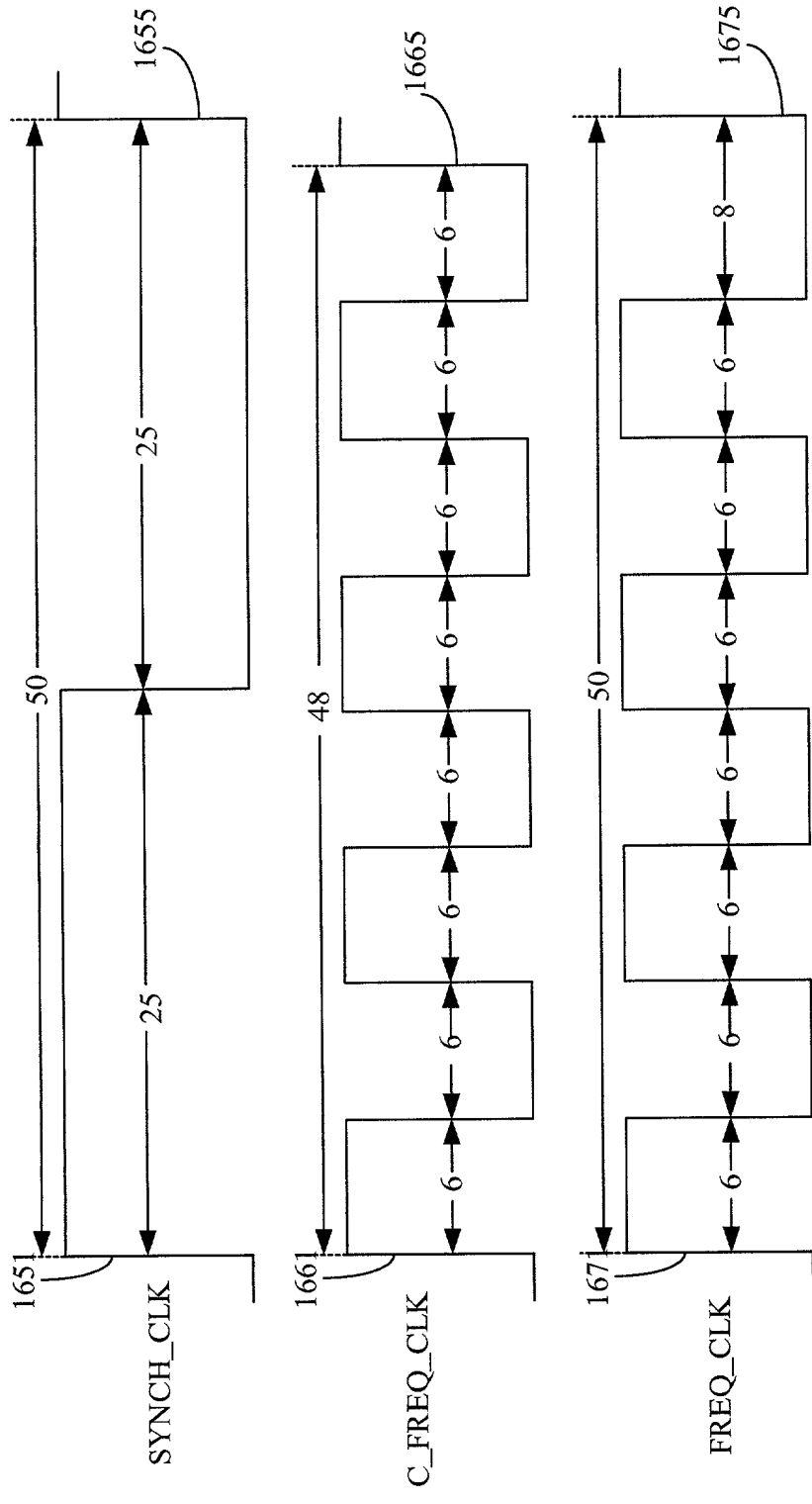


FIGURE 16)

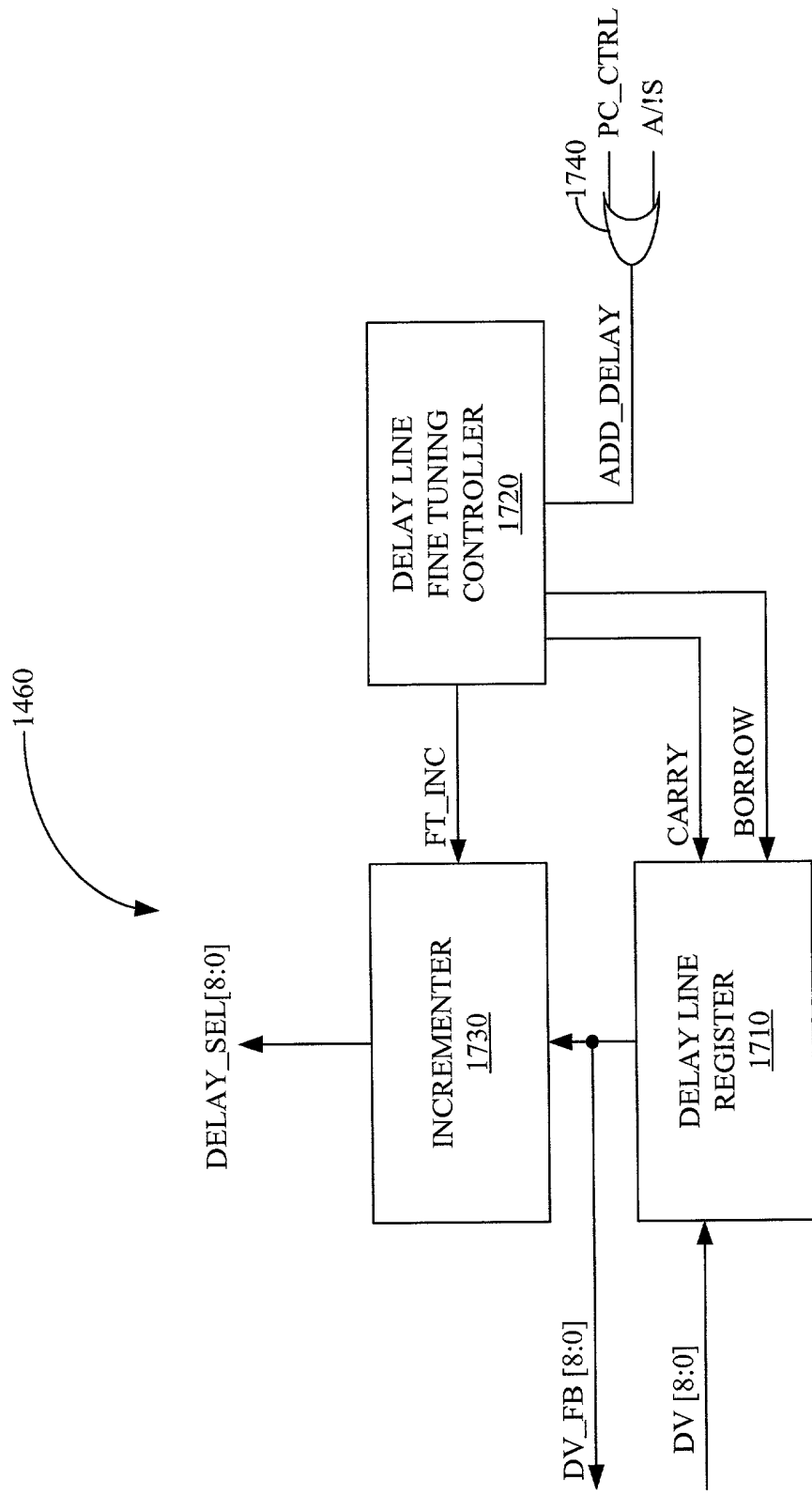


FIGURE 17

000001100000000000000000

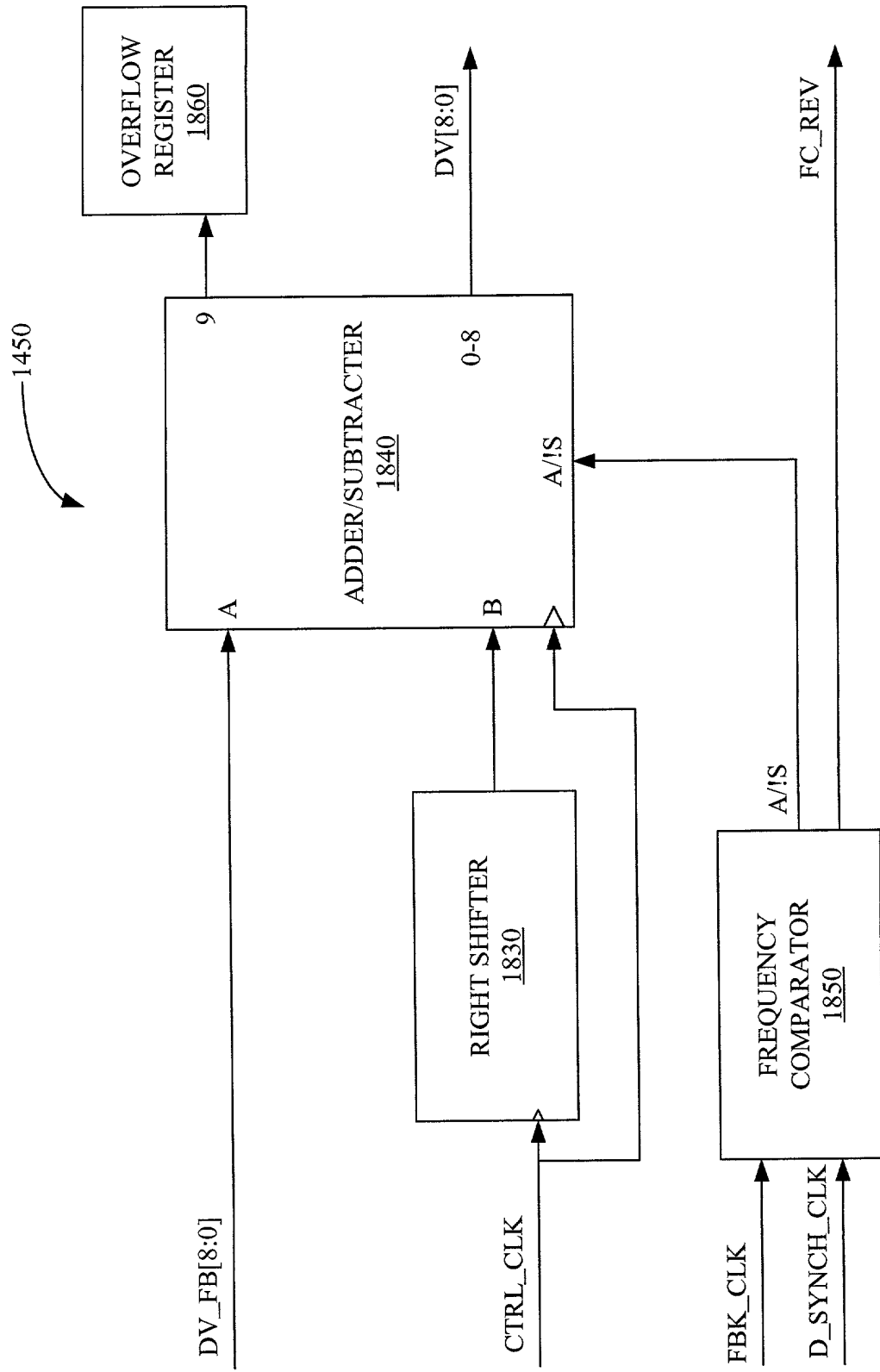


FIGURE 18

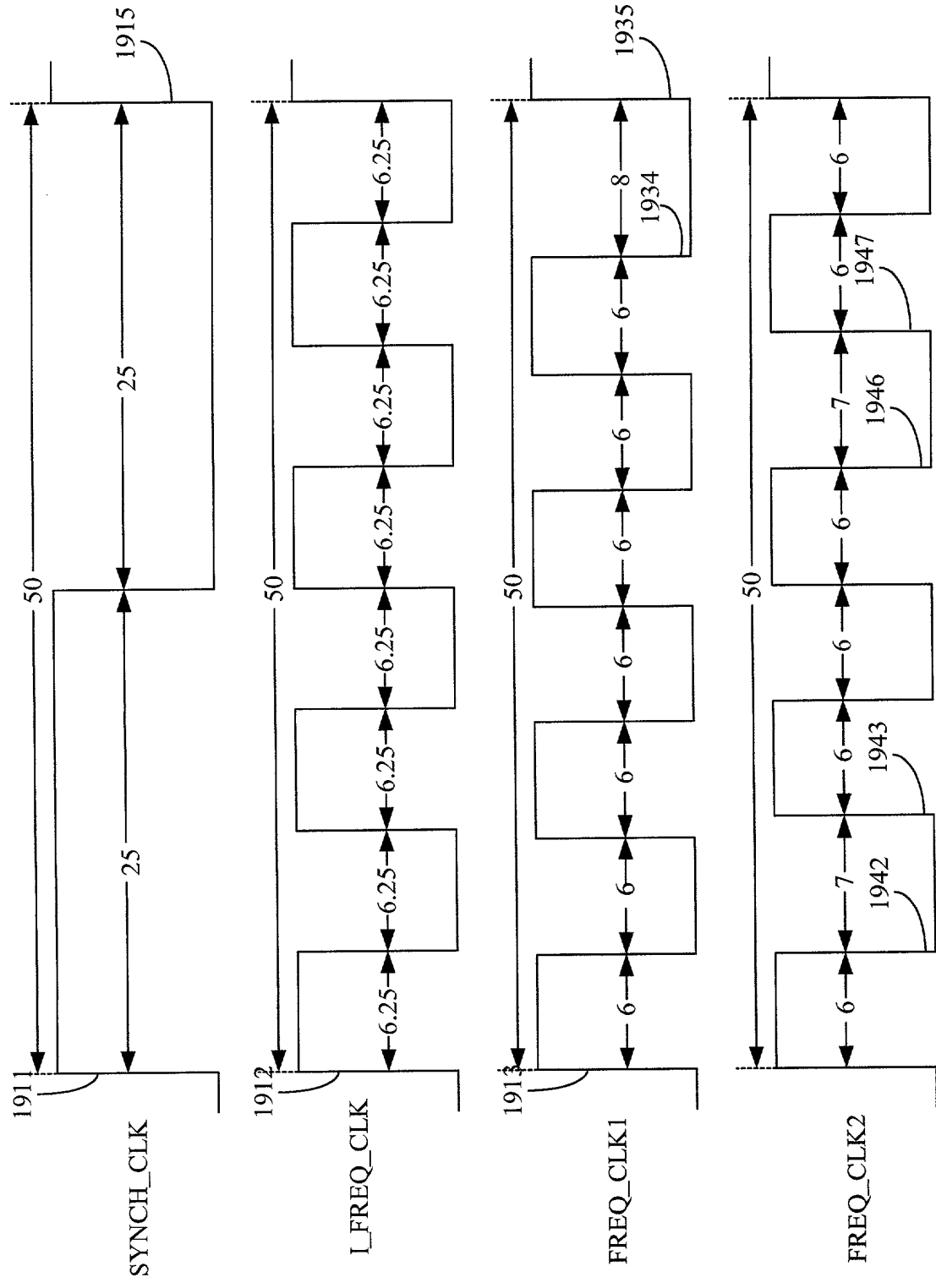


FIGURE 19

FIG. 20

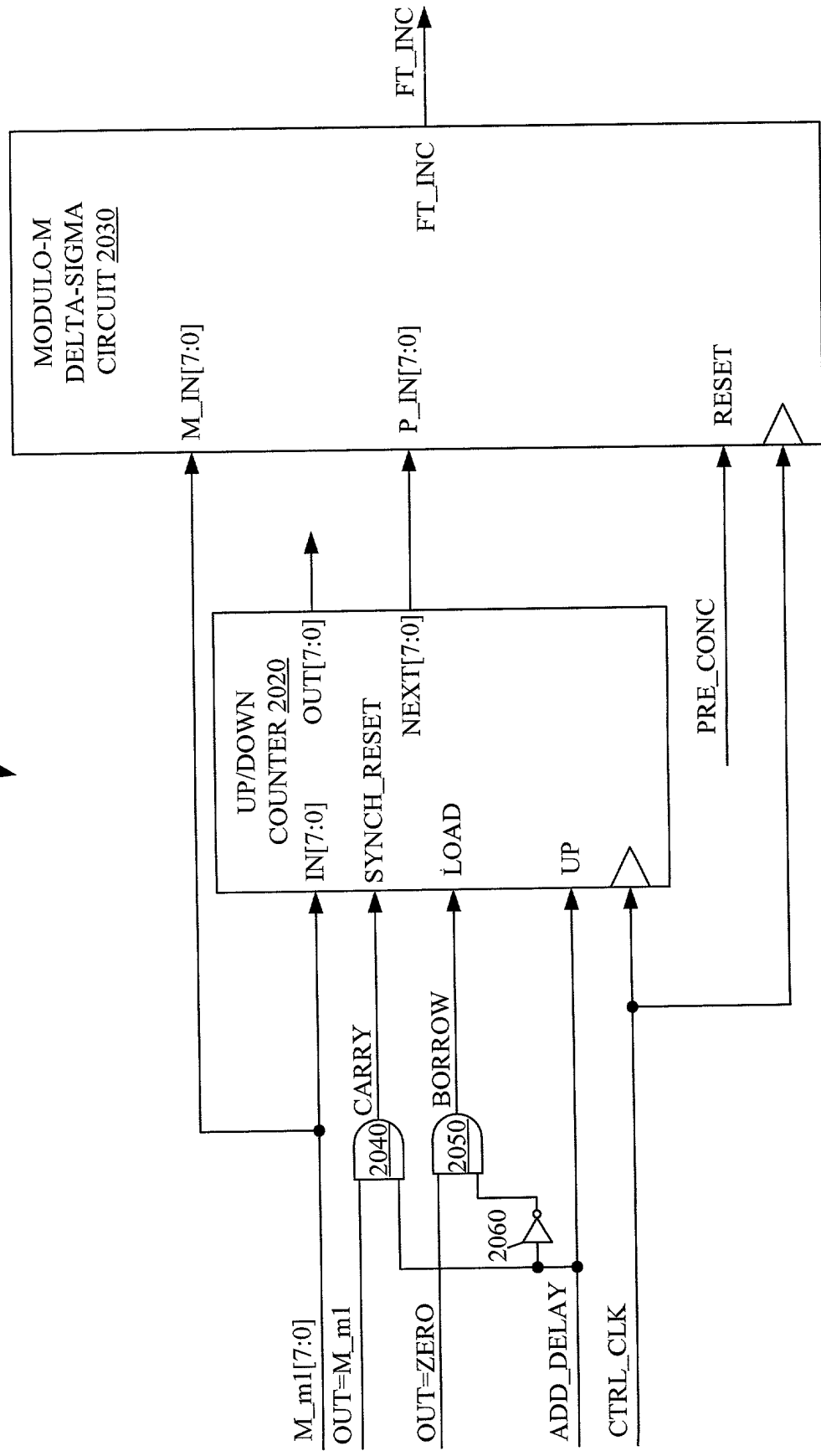


FIGURE 20

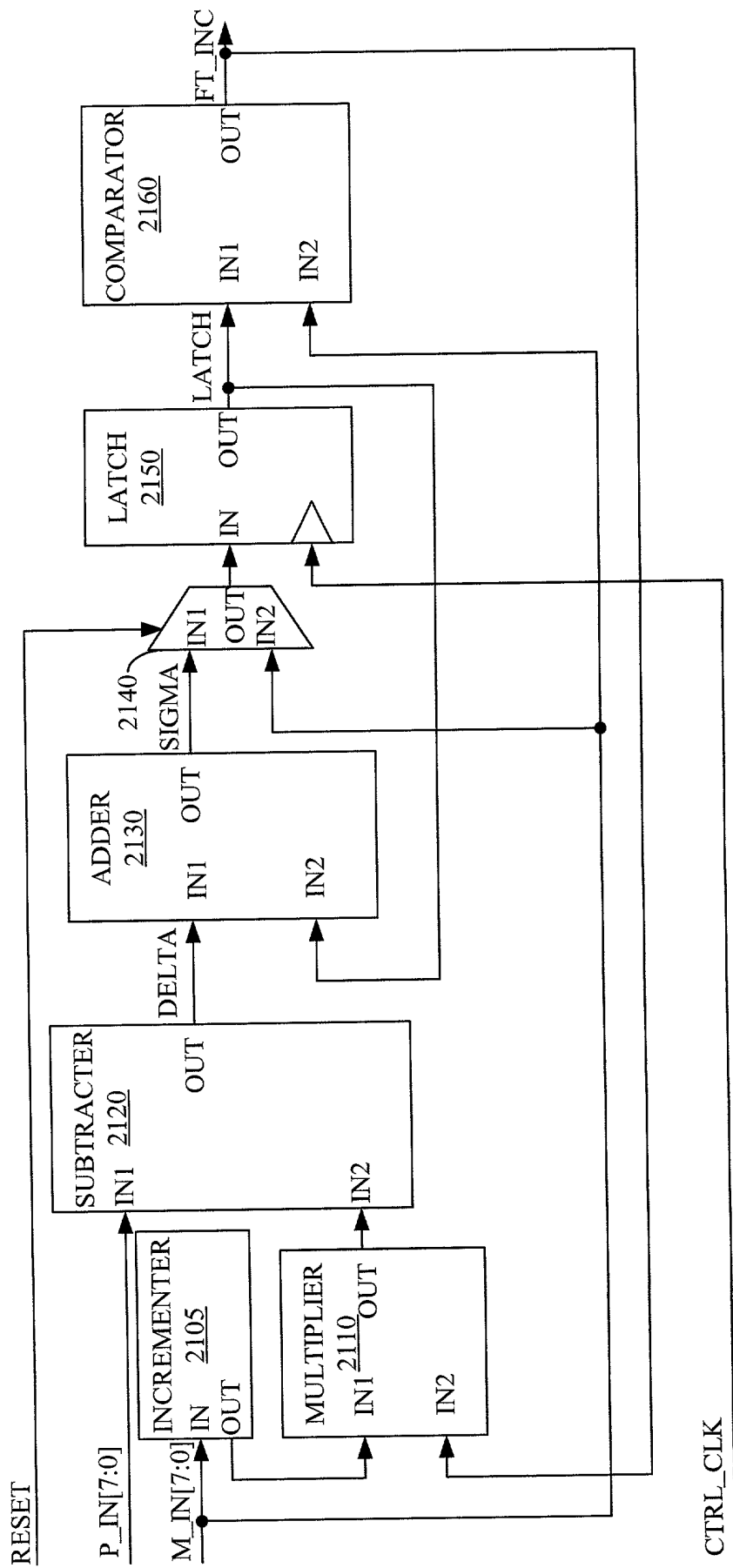


FIGURE 21

DECLARATION FOR PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below adjacent to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of subject matter (process, machine, manufacture, or composition of matter, or an improvement thereof) that is disclosed and/or claimed and for which a patent is solicited by way of the application entitled

SYNCHRONIZED MULTI-OUTPUT DIGITAL CLOCK MANAGER

which (check)

- ☒ is attached hereto.
☐ and is amended by the Preliminary Amendment attached hereto.
☐ was filed on _____ as Application Serial No. _____.
☐ and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified application, including the claims, including portions amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, § 1.56(a).

I hereby claim foreign priority benefits under title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
			Yes	No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)		
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below

_____ (Application Number(s))	_____ (Filing Date (MM/DD/YYYY))
-------------------------------	----------------------------------

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as any subject matter of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56(a) which occurred between the filing date of the prior application(s) and the national or PCT international filing date of this application:

_____ (Application Serial No.)	_____ (Filing Date)	_____ (Status-patented, pending, abandoned)
--------------------------------	---------------------	---

_____ (Application Serial No.)	_____ (Filing Date)	_____ (Status-patented, pending, abandoned)
--------------------------------	---------------------	---

_____ (Application Serial No.)	_____ (Filing Date)	_____ (Status-patented, pending, abandoned)
--------------------------------	---------------------	---

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the United States Patent and Trademark Office connected herewith:

Keith A. Chanroo (36,480), Edel M. Young (32,451), and Lois D. Cartier (40,941) all located at Xilinx, Inc., 2100 Logic Drive, San Jose, California 95124, and Patrick T. Bever (33,834); E. Eric Hoffman, (38,186); Edward S. Mao (40,713); Julie Stephenson (41,330); and Jeanette S. Harms (35,537) all located at Bever Hoffman & Harms, LLP, 2099 Gateway Place, Suite 320, San Jose, California 95110.

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2100 Logic Drive
San Jose, California 95124

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Title 18, United States Code, § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature _____ Date _____

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Inventor's signature _____ Date _____

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Full name fourth inventor _____

Inventor's signature _____ Date _____

Residence _____ Citizenship _____

Post Office Address _____

EMY:pbs